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SPECIAL ROD SYSTEM STUDIES

THIRD QUARTERLY REPORT

IBM

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Special AROD System Studies

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PREPARED FOR

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ABSTRACT

This document is the Third Quarterly Report on NASA Contract No. NAS 8-11050, Special AROD System Studies. This is an interim report on Items 6, 7 and 8 of the Work Statement and is presented in that order although the major effort was devoted to the Phase Lock Loop task.

Section 1 on AROD System Interface Investigations reports on a continuing study of interface considerations between the Saturn V Data Adapter (SVDA) and the AROD sensor. A method of achieving an interface with the Saturn Telemetry System, using capabilities established by the SVDA, is advanced. A major aspect of the interface investigation has been consideration of continuous doppler extraction. Some problems of a fundamental nature have been identified which lead to implementations whose complexity outweigh the advantages of continuous doppler readout from the interface point of view. A proposed laboratory feasibility test setup, implementable with commercial equipment, is discussed as a means of assessing these approaches against the more conventional interval-counting schemes.

In Section 2 (Phase Lock Loop Advanced Circuit Investigations) the bases for establishing an experimental comparative evaluation of L-C vs crystal VFO's for the AROD tracking filter application are presented. In addition, the design considerations leading to the L-C VFO circuit type Phase Lock Loop which has been developed for this evaluation is discussed. Initial work on state control VFO's and a VFO-multiplier circuit developed for application to a type II loop is reported on. The characteristics of type II loops and their impact on the AROD problems of reacquisition after signal fade and tracking phase errors are also discussed.

Section 3 is a preliminary report on the Maxson Electronics subcontract for the study of linear coaxial cavity amplifiers for the ground transponder transmitter. A wideband envelope feedback technique test setup is described,

as is the instrumentation for evaluating the technique. This approach, if successful, would help the severe intermodulation developed by an AROD transponder transmitter chain due to the essentially SSB modulation of the up-link signal. Results obtained to date indicate approximately 5 db improvement in the third-order products relative to open loop operation. The final report on this work will be available by the next monthly report.

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ILLUSTRATIONS

Section 1

AROD SYSTEM INTERFACE INVESTIGATIONS

1.1 SVDA Status for AROD

The status of the Saturn V Data Adapter (SVDA) has not changed materially from that reported upon previously. However, a summary of the SVDA characteristics which impact AROD, as well as those which are impacted by AROD, is appropriate here.

The present clock oscillator stability of 25 parts in 10^6, as well as restricted growth potential for the Real Time Register's delay line mechanization, preclude use of computer real time for AROD measurement timing. This will require that time synchronization between AROD real time and computer real time must be carried out as a computer operation. To facilitate this the AROD real time should be accummulated in natural binary code in some suitable manner from the AROD equipment VMO.

Adequate addressing capability for data inputting still exists. However, since the eight quantities will be time multiplexed out of AROD to conserve inter-connection wiring, a reduction from eight unique addresses to only one would not lead to any difficulty. A fixed format sequence generated by an eight-state counter within the AROD Data Extraction Processing multiplexer control function will suffice.

On the other hand, address availability on computer outputs is restricted and growing smaller. Consequently, a requirement for extensive computer-generated command and control functions will have important impact on the DA. At present, less than six addresses for such use might be made readily available.

The interface is still best approached on a parallel signal transmission basis, with 13-bit channels from AROD to SVDA and 26-bit channels from

SVDA to AROD. While standard transformer coupled circuits may become available in the future, the DIA input "buffer" circuit and the simplex output driver circuit are still the consistent approach, from an equipment point of view, for both sides of the interface. The question of redundancy affects only the interconnecting cabling, i.e., simplex or TMR (Triple Modular Redundancy), since AROD functions themselves will be simplex. For a TMR approach to interconnections, an AROD output driver would be simplex driven at its input and fan to TMR to drive three lines independently. An AROD input "buffer" would, under these conditions, emulate the voting characteristics of a TMR-simplex output driver such as used in the DA.

1.2 Telemetry Interface for Prototype Flight Test

To accommodate the telemetry requirement for the AROD sensor prototype flight test, some form of buffer storage must be provided. Also, since active computer control of the AROD sensor need not be accomplished, some form of permanent storage of station identification and pre-programmed flight path information must be provided. Rather than burden the AROD equipment design with digital data handling tasks, a proposed solution would be to exploit existing SVGC-SVDA capabilities.

For asynchronous access by either computer or telemetry of AROD data extraction outputs, at least four, and possibly eight, additional registers for buffer storage will be required. A completely operational-digital extraction processing technique would, of course, make all eight quantities (and real time—if AROD accummulated) available "on demand"—by either TM or computer. Assuming, however, that doppler continues to be extracted by an absolute (whole number) technique, such as EPUT time encoding; then these four quantities must be buffered in order to implement a "request" interface for TM (or computer). The essential idea is that unused storage slots in the Data Adapter's Data Output Multiplexer (DOM)—a TMR Delay Line buffer storage—be utilized. Non-interfering access to this can be gained by suitable logic and timing between the extraction processing function in AROD and the PIO address decoder in the SVDA. The use of the DA Output Bus as the

transfer path between AROD and the DOM can be established through use of the DIM/Serializer inputting facility at times other than when a PIO input operation is taking place (see Figure 1-1). A similar situation presently exists with respect to use of the DA as a channel between the DDAS (Digital Data Acquisition System) and Saturn Telemetry via the DOM in the orbital checkout mode. To accommodate ten or more 26-bit quantities at four frames a second data rate would not impose any great strain, since the computer does not see this information at any time—the transfers taking place during non-PIO instruction times.

The major benefit to be derived from this suggested approach stems from the utilization of an existing, established interface with an asynchronous telemetry system for purposes of word formatting, timing, validity and parity bit generation. The data flow direct to telemetry from an AROD sensor prototype would be subject to the same constraints as are already solved by the DA-TM interface. Only for the all-operational, digital extraction approach could an asynchronous interface with TM be configured on an "instantaneous" access request basis.

A further aspect to utilization of the SVDA in flight test relates to ready availability of storage pertaining to programming control of the ground stations. Access to such information stored within the SVGC duplex memory via the DA is not particularly difficult. However, in this case a PIO instruction must be designated to output to AROD an addressed 26-bit word from memory via the DA Buffer Register. This is shown in Figure 1-1.

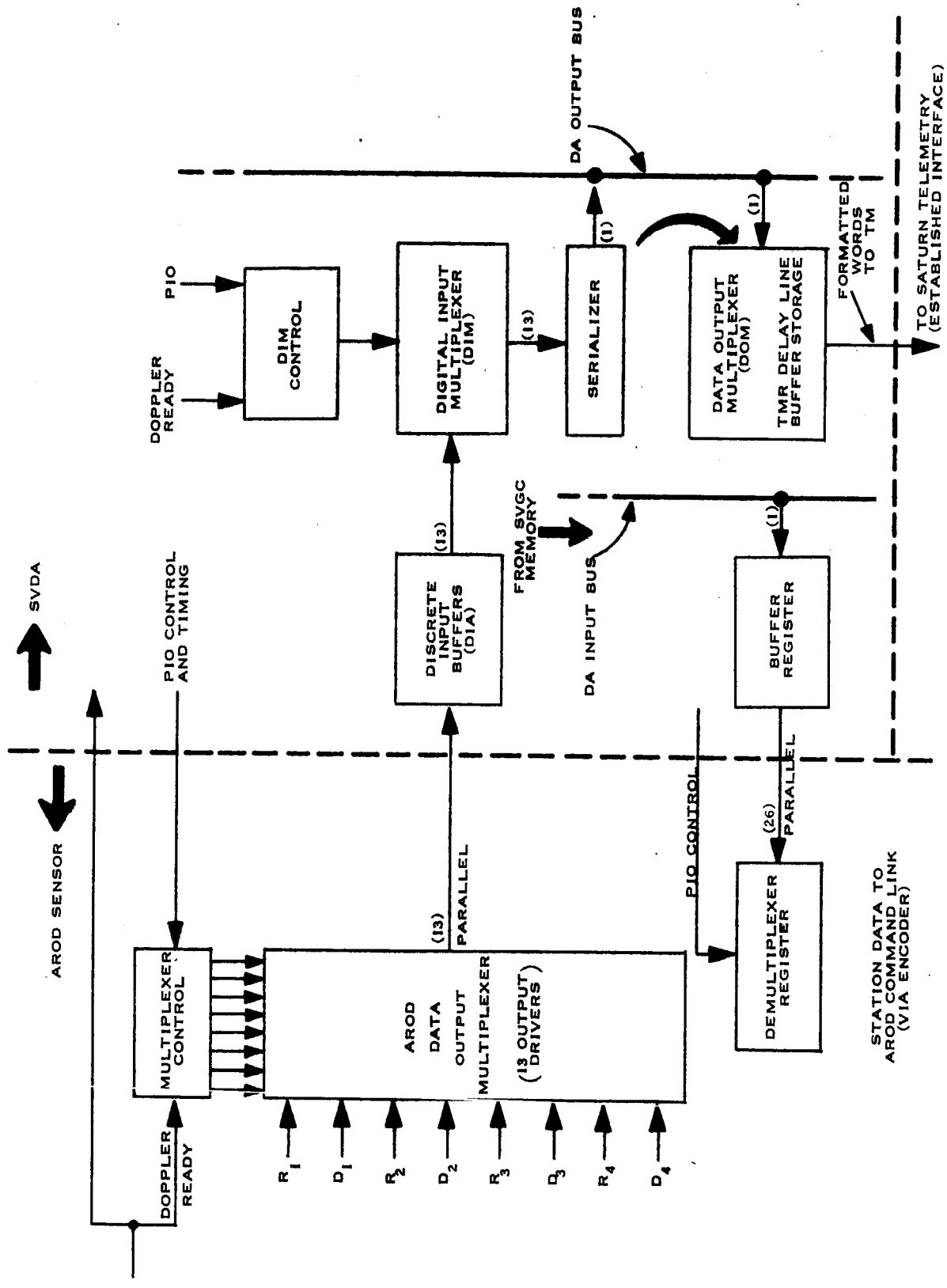


Figure 1-1. Suggested Prototype Flight Test TM Interface

1.3 Continuous Doppler Extraction

The problem of achieving a continuous "readout" or extraction of the doppler shift in frequency still appears to have no simple solution from the point of view of a space-worthy hardware implementation. The difficulty is largely due to the need for establishing a highly accurate, fine resolution synthesis of frequency not dependent upon analog-analog conversions.

A primary issue is whether the continuous extraction of doppler to a 1 part in 10^6 accuracy is worth the trouble, even if implementable with no more complexity than an absolute (or whole number) time encoding method of the usual EPUT-type, plus a suitable buffer storage register with the appropriate number of bits and associated gating. The basic contention of the absolute counting method is that even though a relatively long time is taken to carry out the counting process the value obtained corresponds to an average value which was the "instantaneous" value of frequency at the midpoint in time of the doppler counting interval. This is based on the fact that the $\ddot{R}$ or doppler rate term is sufficiently constant over this interval for all trajectories to maintain the resulting interpolation error negligible. For a maximum doppler rate of 5KHz per second at the zenith of the lowest orbit, and the system requirement of 1Hz in frequency resolution, the element having this resolution must change within 20 sec in order to follow the input frequency. However, the accuracy of a simple cycle counting method in the face of such high doppler rates also merits questioning. For cycle counting over an observation interval of 250 msec the frequency can only be determined to within 4Hz. Obviously this can be improved with interpolation. This is true regardless of the method of encoding since it follows directly from inverse time-frequency domain relationships. Fundamental to the counting method is the taking of an independent sample of limited duration of a continuous time function, namely a quarter-second "look" at a continuous variation of range rate. On the other hand, a mechanization which maintains "track" with the physical variable is not subject to this consideration, except insofar as lags are encountered in keeping up

with the variable dynamics. It may be argued that the high digital resolution of a limited time aperture sampling process can only be achieved by an interpolation within the above physical limit. The continuous extraction approach benefits from a continuously increasing sampling time aperture from the point of view of this fundamental limitation. The limitations imposed on a continuous extractor by variable dynamics can also be overcome with an interpolation method similar to the absolute sampling case.

Of the variety of ways which suggest themselves to achieve a continuous measure of a changing frequency, the approach having the most likelihood of success is based on use of frequency synthesizer as a precision digital-to-analog (frequency analog) converter. Admittedly, this method suffers from considerable complexity. However, the synthesizer approach does permit a ready evaluation of feasibility in the laboratory by using various commercially available "digital" synthesizers, such as the HP 5100A/5110A or GR 1162A. A scheme based on the HP unit, which has 1 msec maximum switching time from one frequency to any other frequency from 0 - 50 mc., is shown in Figure 1-2.

This approach uses the synthesizer as a D/A converter. The technique of using a D/A converter in a feedback configuration to achieve an A/D conversion is a very common technique widely used in voltage-to-digital conversion. The essential difference in this case is the use of a multiplier for the feedback loop comparator. When the input and synthesizer output frequencies are equal, the multiplier acts as a phase detector. The control unit interprets the direction of change of phase as the input frequency begins to change, to generate either an up or down increment to the binary coded decimal, or decimal, organized bidirectional counter. BCD, or decimal, counters with 5 to 20 KHz maximum counting speeds are widely used in instrumentation and process control and are readily available. A decimal unit would obviously eliminate the BCD/decimal decoding function. It is suggested that such a setup may be readily implemented to test the feasibility of continuous extraction techniques. The results of such a test will serve to settle some of the fundamental issues as well as generate requirements for a synthesizer equipment approach optimized particularly for AROD extraction requirements.

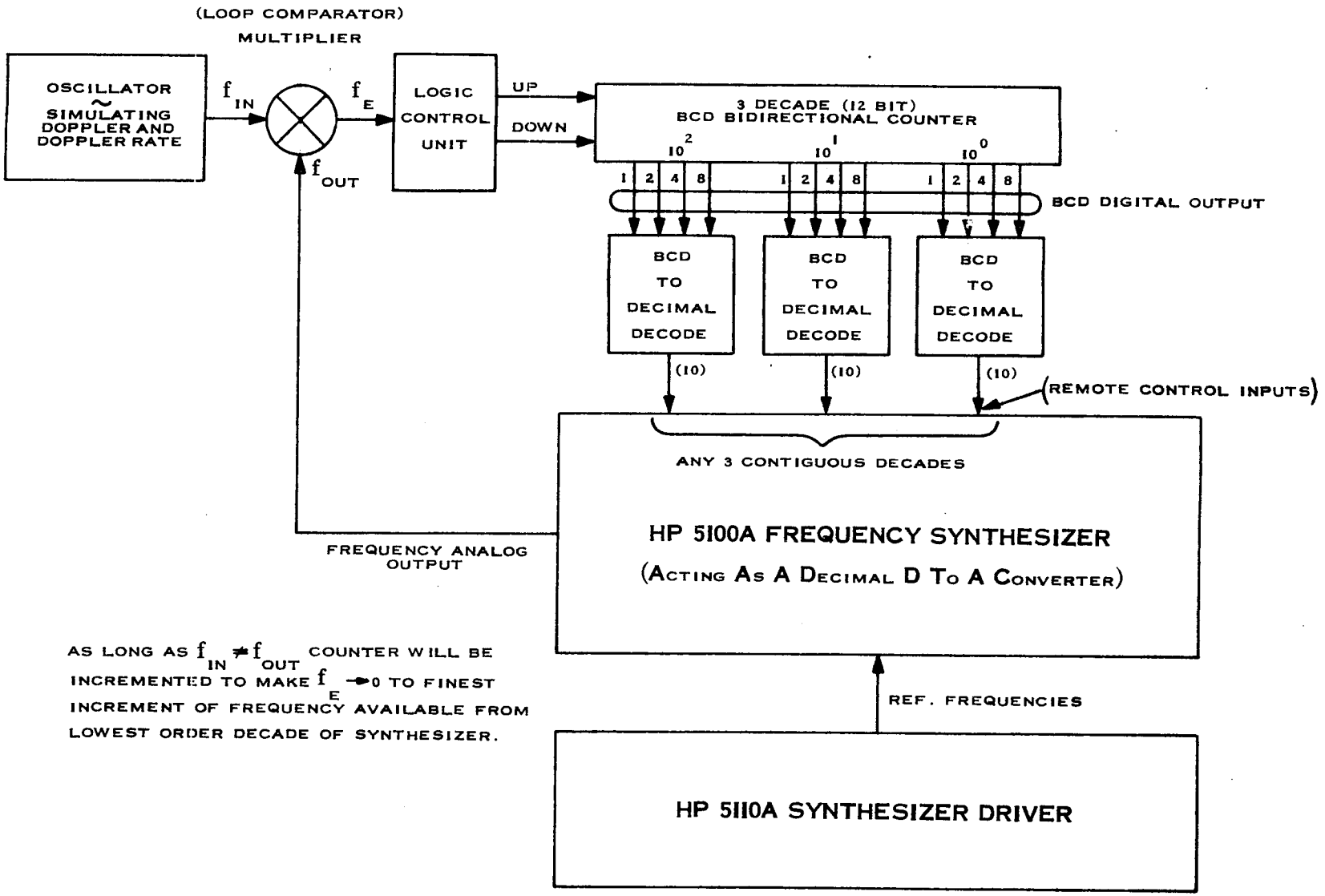


Figure 1-2. Laboratory Feasibility Setup for Continuous Doppler Extraction

Section 2

PHASE LOCK LOOP ADVANCED CIRCUIT INVESTIGATIONS

2.1 Comparative Evaluation of Oscillator Phase Noise in Tracking Loops

The variable frequency oscillator of a phase locked loop is the major contributor of the loop internal phase noise, and it should therefore exhibit a high phase stability to minimize system errors. Since the oscillator's phase noise errors depend not only on the type of circuitry used but also on the frequency of operation, a design choice will have to consider the AROD tracking system configurations. To evaluate the phase noise contribution for a particular system configuration, a performance comparison for different types of oscillators will first be made.

A commonly used measure of performance of an oscillator is its coherence time, which is defined as the time interval for which the standard deviation of the oscillator phase change is equal to one radian. A highly stable oscillator, whose phase noise is small, will therefore have a high coherence time.

Several studies have been made in this area and no attempt will be made to derive the formulas obtained in references 1, 2 and 3. Some of the more important aspects of coherence time will be repeated and used to calculate the highest possible coherence time in practical oscillators. The values thus obtained will then be used to indicate optimum tracking loops for the AROD System.

2.1.1 General

It has been shown [1, 2, 3] that the output of an oscillator is not a pure sine-wave, owing to the thermal noise generated in the circuit elements. The output spectrum, as observed by a spectrum analyzer, will appear to have a single large peak of extremely narrow bandwidth in addition to a low level, wideband envelope ("background") noise. The relationship between the power levels of the narrow band phase noise and the wideband envelope noise is given by [1, 2, 3]

$$\frac{\Delta\omega}{\partial\omega} = \frac{1}{2\pi}\,\frac{P_S}{P_N} = \frac{SNR}{2\pi} \qquad (2\text{-}1)$$

with $\Delta\omega$ = bandwidth of envelope noise rad/sec

$\partial\omega$	=	bandwidth phase noise	rad/sec
P_S	=	power of carrier signal	watts
P_N	=	power of background noise	watts
SNR	=	signal-to-noise ratio	

It has further been proven that the coherence time τ_c is equal to the reciprocal of the phase noise bandwidth, or

$$\tau_c = \frac{SNR}{2\pi\Delta\omega} = \frac{Q}{2\pi\omega_o} \cdot (SNR) \qquad (2\text{-}2)$$

This formula is (except for a factor of 2) identical to Edson's equation 52 where he assumes the thermal noise to be solely contributed by the oscillator's tuned circuit. For this the SNR is given by

$$(SNR)_{t.c.} = \frac{P_o}{kT\Delta f} \qquad (2\text{-}3)$$

with

P_o	=	power in tuned circuit	watts
k	=	Boltzmann's constant	wattsec/^{o}Kelvin
T	=	temperature	degrees Kelvin
Δf	=	bandwidth	cycles/sec

The SNR at the input of the amplifying element is further determined by the amount of power delivered to this input by the tuned circuit and by the noise figure F of the amplifying element, or

$$(SNR)_{in} = \frac{\beta\ P_o}{kT\Delta fF} \qquad (2\text{-}4)$$

In a commonly used circuit as shown in Figure 2-1 (modified Colpitt for high L-C ratio [4]), the factor depends on the impedance ratio between load and tuned circuit and on the stepdown ratio of the two capacitors, C_1 and C_2.

Edson[1] has indicated that, due to nonlinear limiting effects in the amplifier, the performance is worsened by a factor S which is in the order of 5 to 10 in typical oscillators. Using this parameters S, and combining equations 2 and 4, gives

$$\tau_c = \frac{\beta P_o Q^2}{kTFS\omega_o^2} \qquad (2\text{-}5)$$

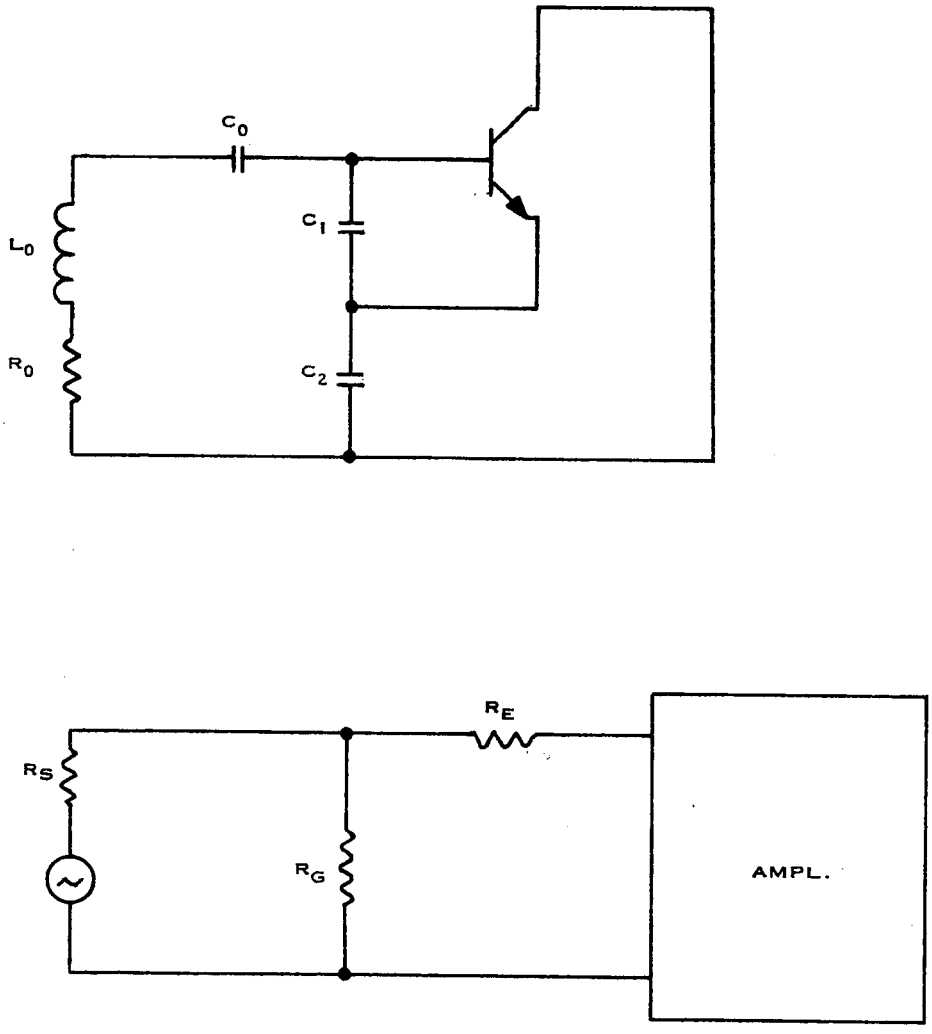


Figure 2-1. Noise Figure Equivalent Circuits

with

τ_c	= coherence time	secs.
β	= ratio of input power to tuned circuit power	
P_o	= power in tuned circuit	watts
Q	= selectivity of tuned circuit (including loading effects)	
k	= Boltzmann's constant	wattsec/degree K
T	= absolute temperature	degrees Kelvin
F	= noise figure	
S	= limiting factor	
ω_o	= oscillator frequency	rad/sec

It is now obvious that in order to obtain a high coherence time and low phase noise at a given frequency that the power and the loaded Q of the tuned circuit should be as high as possible, while the noise figure (and S) should be kept to a minimum.

Other formulas useful in determining the coherence time from particular measurements are

$$\tau_c = \frac{1}{S_o^2 \omega_o^2 \tau} \tag{2-6}$$

and

$$\tau_c = \frac{\tau}{\phi_n^2} \tag{2-7}$$

with

S_o	=	short-term phase or frequency stability, measured over a time interval τ
ϕ_n	=	rms phase noise measured in a radian bandwidth $1/\tau$

2.1.2 Noise Figure Calculations

Since the noise figure of the oscillator's amplifying element is of significant importance in obtaining a high coherence time it is important that amplifier selection and impedance matching be done carefully. In the simplified circuit of Figure 2-1, the noise figure can be calculated.
Thus:

$$F = 1 + \frac{R_s}{R_G} + \frac{R_e}{R_s}\left(1 + \frac{R_s}{R_G}\right)^2 \qquad (2\text{-}8)$$

with

R_s = source impedance

R_G = input impedance

R_e = equivalent noise impedance

In the problem under discussion the source impedance R_s is the stepped-down impedance of the tuned circuit at resonance.

By defining two parameters

$$x = \frac{R_s}{R_G}$$

and

$$y = \frac{R_e}{R_G}$$

equation (2-8) becomes:

$$F = 1 + x + \frac{y}{x}(1 + x)^2 \qquad (2\text{-}9)$$

Figure 2-2 displays a plot of the noise figure as a function of x with y as independent variable.

This graph shows that the optimum noise figure is obtained for a lowest possible y, while for any given y the required x is always less than or equal to 1.

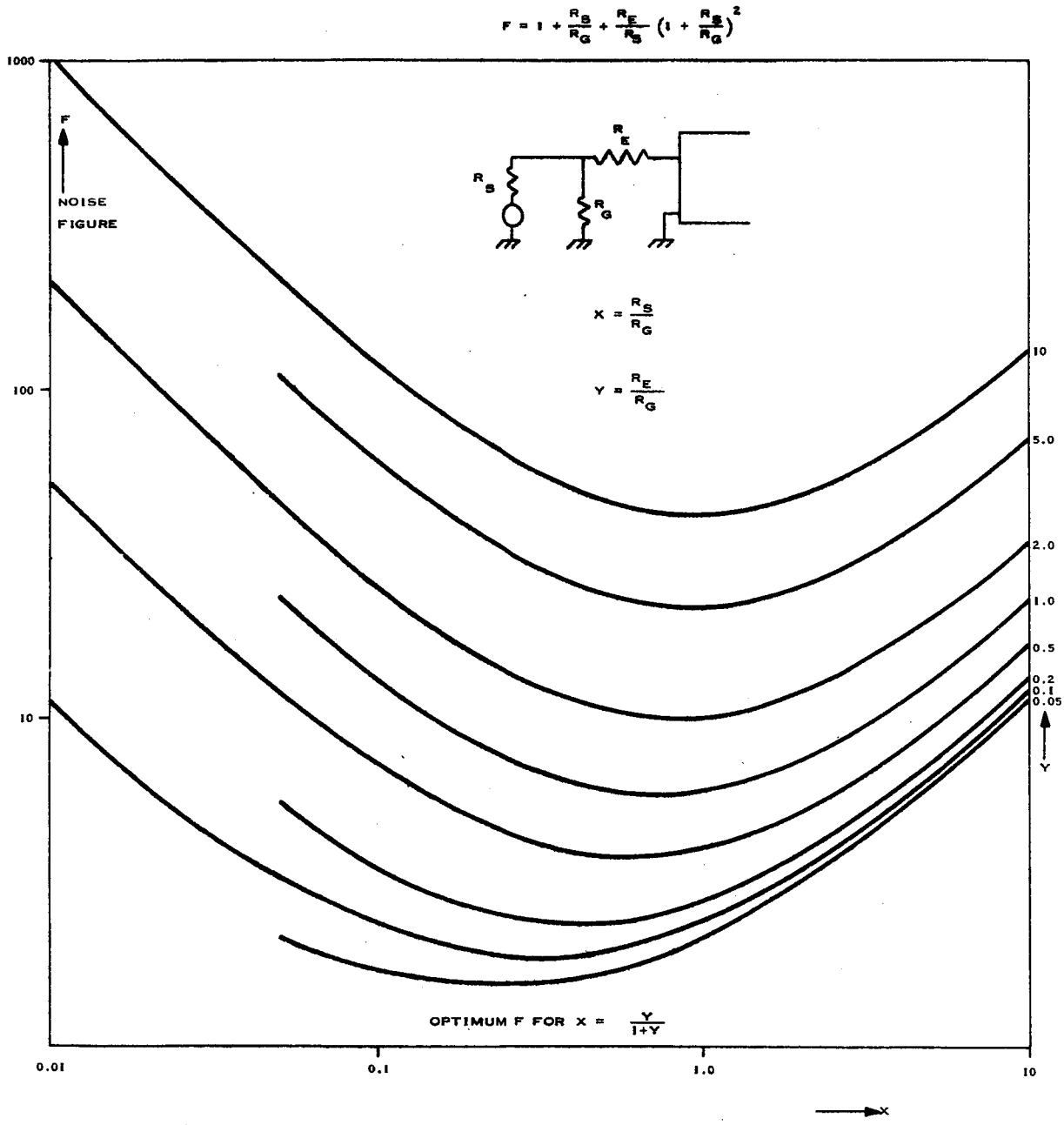


Figure 2-2 Noise Figure as a Function of Relative Source Impedance and Relative Equivalent Noise Impedance

It should be noted that the y is a known parameter for any amplifying element or can be calculated from its published data. In general, y will be much lower for vacuum tubes than for transistors, and will, for a low noise vacuum tube, be considerably less than 0.1.

For transistors, which will be considered here, the y parameter can be anywhere from 0.05 to well over 10, and will depend on operating frequency. Some typical low noise transistors, as the 2N918 or the 2N1141, have a y of 0.1 at 5 Mc/s. It is important to realize that a low equivalent noise resistance is only valuable inasmuch as more external loading can be used, but it does not improve the noise figure.

The input impedance R_G will effectively load down the tuned circuit and lowers its Q by a factor $\frac{1}{1+x}$. Also, the power delivered to the input impedance is equal to the source power multiplied by a factor of $\frac{x}{1+x}$. Using the values of noise figure F, circuit Q and power ratio in equation 2-5 and assuming the use of a transistor with a low parameter y, it can be found by differentiation that the maximum coherence time is obtained for a value of x = 0.5. Equation 2-5 then becomes, with y = 0.1 and S = 5:

$$\tau_{c_{max}} = 3 \times 10^{18} \frac{P_o Q_o^2}{\omega_o^2} \qquad (2\text{-}5a)$$

2.1.3 Fixed Frequency Crystal Oscillator

With the observations made in section 2.1.1 the maximum coherence time for a fixed frequency crystal oscillator can be calculated. The circuit diagram shown in Figure 2-1 will be used as a representative circuit. In this circuit L_o and R_o represent the crystal inductance and series resistance while C_o is the crystal series capacitance. C_1 and C_2 are impedance matching capacitors whose ratio also determines the feedback ratio. C_1 is usually 5-20 times larger than C_2. Supply circuitry is not shown but the circuit can be grounded at either the base or the emitter.

From the transistor specifications the optimum source resistance can be determined. As an example for the low noise transistor 2N918 with R_e = 150 ohms and R_g (loaded) = 750 ohms, y = 0.2 and with x = 0.5, R_s = 375 ohms. Since the impedance of the tuned circuit is stepped down by a factor $(C_o/C_1)^2$, the value of C_1 can be calculated from:

$$\left(\frac{C_o}{C_1}\right)^2 \quad Q_o^2 \quad R_o = R_s$$

or

$$C_1 = Q_o \; C_o \left(\frac{R_o}{R_s}\right)^{1/2} \qquad (2\text{-}10)$$

If further C_2 is selected to be $C_2 = 0.1\ C_1$ to set the transistor gain at 10, the basic circuit design is completed.

The coherence time τ_c can now be calculated with equation 5 and some crystal data available from the manufacturers. Crystals are presently available with a selectivity Q_o as high as 10^6 at 5Mc/s but extreme care must be exercised to limit the power dissipated. The recommended power should be less than 1 microwatt.

Then with $Q_o = 2 \times 10^6$

and $P_o = 2 \times 10^{-7}$ a watt

Equation (5a) gives:

$$\tau_c = 2.5 \; 10^{24} \times \frac{1}{2} \quad \text{o}$$

at 5 Mc/s this gives

$$\underline{\tau_c = 2.5 \times 10^9 \text{ secs}}$$

It is interesting to compare this value with that obtained with some existing, standard oscillators.

The Hewlett Packard Model 104 AR has some excellent data from which the coherence time can be determined. The short term stability is given as 3×10^{-11} for 1 sec intervals, or with equation 6, at 5 Mc/s:

$$\tau_c = \frac{1}{S_o^2 \omega_o^2 \tau} = 10^6 \text{ secs}$$

The phase noise is given as 1.5×10^{-4} radians rms in a 6 cps bandwidth or with equation 7:

$$\tau_c = \frac{\tau}{\phi_n^2} = \frac{1}{2\pi B \phi_n^2} = 1.2 \times 10^6 \text{ secs}$$

The power ratio (SNR) at 5 Mc is given as 89 db, or with equation (2-2):

$$\tau_c = \frac{Q}{2\pi\omega_o} \text{ (SNR)} = 6 \times 10^6 \text{ secs}$$

Since this coherence time is about 1000 times worse than should be obtainable, it is of interest to examine the circuitry closely. From this it can be learned that the crystal resonance impedance is stepped down to a far lower value than is desirable to obtain a high SNR at the input of the transistor; and it is estimated that y and x (as defined in Section 2.1.2) are 2 and 0.01 respectively. The noise figure is therefore about 200, or 100 times worse than assumed, while the available power is one order of magnitude lower. For the AROD application it should be possible to improve the performance of this oscillator by selection of a low noise transistor and by proper matching techniques.

2.1.4 Fixed Frequency L-C Oscillator

Similar calculations can be made for the impedance matching networks for the L-C oscillator, as have been made in Section 2.1.3. If for instance the Q of the

coil is 100 a simple circuit can be made with L_o = 8.2 μ H, C_o deleted, C_1 = 1200 pF and C_2 = 133 pF.

The coherence time is again limited by the power. While the power had to be very low in the crystal oscillator case in order to prevent damage to the crystal itself, in the L-C type oscillator it has to be reasonable in order to prevent damage to the transistor. With a tuned circuit power of 10^{-3} watts, the coherence time at 5 Mc/s becomes

$$\tau_c = 3 \times 10^{18} \frac{P_o Q_o^2}{\omega_o^2}$$

$$\underline{\tau_c = 3 \times 10^4 \text{ secs}}$$

2.1.5 Variable Frequency Crystal Oscillator

In this and in the next section it will be assumed that the frequency of the oscillator is changed by means of a variable capacitance diode ("varicap" or varactor diode) and controlled by the back voltage applied to this diode.

It will now be shown that the maximum obtainable coherence time is to a large extent determined by the maximum permissible frequency deviation of the basic oscillator frequency and by the implementation and characteristics of the varactor. The crystal oscillator frequency can only be deviated a small amount without a rapid deterioration of its Q or to prevent discontinuation of the oscillations, due to the high ratio of parallel-to-series capacitance.

Assume:

maximum allowable frequency deviation = $\pm$ n %

Then

total required capacity change of tuned circuit = $\pm$ 2 n %

If

total control range of the varactor's capacitance = $\pm$ m %

Then

$$\frac{\text{C tuned circuit}}{\text{C varactor}} = \frac{m}{2n}$$

The tuned circuit impedance is then transferred to the varactor by the square of this ratio or with $(m/2n)^2$, and this transformed impedance will have to be much lower than the total varactor impedance to prevent loading of the tuned circuit. Or:

$$Q_o^2 R_o \left(\frac{2n}{m}\right)^2 << R_v \qquad (2\text{-}11)$$

with $Q_o^2 R_o$ representing the impedance of the tuned circuit at resonance and R_v the total varactor impedance. R_v consists of the equivalent parallel impedance due to the Q of the varactor ($R_p = Q_v \omega_o C_v$) and the driving impedance from the control voltage (effectively in parallel with R_p). This driving impedance has to be limited to prevent varactor leakage current changing the capacitance and consequently the frequency, and also to limit the thermal noise present in this impedance. While at present a high Q and a very low leakage are not simultaneously available in varactors, it is advantageous to select a high Q component. A numerical example will now be given. For high Q crystals the frequency deviation is limited to $n = \pm 0.01\%$ while the control range of the varactor should be kept below $m = 20\%$ to ensure fairly linear frequency control. If a varactor is selected with a $Q_v = 200$ and $1/\omega_o C_v = 2000$ ohm, the equivalent parallel impedance $R_p = 4 \times 10^5$ ohm. Selecting a drive impedance $R_d = 4.10^5$ ohm (with a $\Delta I_{co} = 10^{-6}$ A, the voltage change is V = 0.2 V.) the total varactor impedance is $R_v = 2 \times 10^5$ ohm. Therefore, equation (2-11) gives, with a crystal series resistance of 5 ohm:

$$Q_o << \frac{m}{2n} \left(\frac{R_v}{R_o}\right)^{1/2} \qquad (2\text{-}11a)$$

or

$$Q_o << 2 \times 10^5$$

From this it can be seen that an extremely high quality crystal is of little use in this circuit, since the performance (and coherence time) of the oscillator is to a very large extent determined by the total varactor impedance. It may appear from

equation (2-11a) that a reduction of n is advantageous, since a higher Q would then be obtainable and consequently a higher coherence time (see equation (2-5). However, the reduction in frequency deviation would necessitate an equal amount of frequency multiplication to re-obtain a required deviation, which consequently reduces the coherence time by an equal amount. The net result would be that the eventual coherence time is independent of the selected initial frequency deviation n. If the crystal Q_o is selected to be 8×10^5 the loaded Q is 1.6×10^5. This value can now be used in equation (2-5), assuming optimization of all other circuitry (see Section 2.1.3):

at 5 Mc/s

$$\tau_c = 3 \times 10^{18} \frac{P_o Q_o^2}{\omega_o^2}$$

$$\underline{\tau_c = 1.5 \times 10^7 \text{ secs}}$$

This value of coherence time must be considered as the high limit for an oscillator at 5 Mc/s with a frequency deviation of $\pm$ 0.01% (or $\pm$ 500 cps). A reduction of a factor of 2 in frequency deviation would allow a 4 times higher coherence time; but frequency multiplication of 2 would produce the same coherence time as before. It is therefore desirable to use the highest possible crystal frequency deviation to avoid the complexity of frequency multiplication. A comparison with a commercial unit can be made. The data for the Resdel voltage controlled crystal oscillator model 90814 indicate an equivalent coherence time at 5 Mc/s of 7.2×10^5 secs, with a frequency deviation of 0.015%. Equations (2-11) and (2-5) indicate that the design of this unit would have obtained a coherence time of 1.6×10^6 secs for a deviation of 0.01%. This oscillator's design can therefore be considered close to optimum.

As a final check on the circuit the voltage across the varactor has to be considered. For the numerical example of $P = 2 \times 10^{-7}$ W and R_o = 5 ohm, the voltage across the inductance is $V = Q (P_o R_o)^{1/2}$ = 2000 volts rms. The voltage across the varactor would therefore be, with $\frac{m}{2n}$ = 1000, equal to 2 volts rms, which could be considered acceptable. The voltage on the varactor is a further limitation on the power generated.

A wider frequency deviation is obtainable from a crystal oscillator by reducing the phase vs frequency slope of the crystal. Since this is identical to a reduction in Q, the phase noise (coherence time) will be the same as for a design using a high Q crystal oscillator followed by frequency multiplication. The advantage of the loaded Q crystal oscillator is the reduced system complexity.

2.1.6 Variable Frequency L-C Oscillator

The effect of loading on the tuned circuit by the impedance of the varactor circuit depends on the required rather than on the possible frequency deviation and will be less severe than in the case of the crystal oscillator. If for instance the required frequency deviation n = $\pm$ 2% and the varactor's capacitance is again deviated by $\pm$ 20%, then equation (2-11a) given for the Q of the L-C circuit:

$$Q_o << 5\left(\frac{R_v}{R_o}\right)^{1/2}$$

Using the same value for R_v as in Section 2.1.5 and assuming R_o = 2.65 ohm (as in Section 2.1.4) then

$$Q_o << 1370$$

The circuit suggested in Section 2.1.4 would therefore be very adaptable to introduction of frequency control since the Q of the coil is assumed to be 100. The maximum coherence time of the variable frequency L-C oscillator is consequently nearly the same as that of the fixed frequency L-C oscillator. Considering the small loading effect of the varactor circuit, the coherence time is, at 5 Mc/s:

$$\underline{\tau_c = 2.5 \times 10^4 \text{ secs}}$$

It should be noted that this coherence time is relatively independent of required frequency deviation.

If an L-C oscillator is used in the tracking loop the operating frequency can be chosen as low as 1 Mc/s while still maintaining the required frequency range. From Section 2.1.6 it can be seen that a coherence time of 10^5 secs should be obtainable at 2.5 Mc/s. It is therefore possible to use an oscillator, optimized for long term stability while maintaining low phase noise with little difficulties. The loop will, besides the oscillator, only consist of a phase detector to mix the incoming information with the L-C oscillator and an active filter-operational amplifier combination to obtain the required loop gain and response.

If a crystal oscillator is used in the tracking loop, frequency multiplication is required to obtain the specified frequency range, even when a "Q-spoiled" crystal is used. The signal is mixed with the multiplied crystal frequency and the output of the mixer passed through an IF section. A reference source is then required to phase compare the IF frequency in a phase detector. The loops is then completed with an active filter-operational amplifier combination to obtain the required loop gain and response. The addition of a multiplier, a mixer, an IF section, and a reference frequency source are necessary due to the low frequency deviation capabilities of a crystal oscillator. It should be noted that the IF gain does not reduce the required DC loop gain, but should be sufficiently high to ensure adequate phase detector level.

The maximum obtainable coherence time for the crystal oscillator loop can be calculated from Section 2.1.5. If n is the required percent frequency deviation, or $n = \frac{\Delta\omega}{\omega_o} \times 100$, then the coherence time after multiplication can be calculated from:

$$\tau_c = 3 \times 10^{18} \frac{P_o Q_o^2}{\omega_o^2} \left(\frac{0.01}{n}\right)^2$$

$$= 3 \times 10^{10} \frac{P_o Q_o^2}{(\Delta\omega)^2}$$

For the values of P_o and Q_o given in Section 2.1.5 and for the AROD frequency range of $\pm$ 125 kc/s, the crystal loop coherence time is 85 secs maximum. Since the maximum coherence time is less than two orders of magnitude and thus the minimum phase noise less than one order of magnitude better than required,

The voltage across the varactor can be calculated as in Section 2.1.5 With $m/2n = 5$ and $V_1 = Q\,(P_o\,R_o)^{1/2} = 5.15$ volts rms, the voltage on the varactor is about 1 volt rms.

2.1.7 Comparison between Variable Frequency Oscillators

From Sections 2.1.5 and 2.1.6 it can be seen that the coherence time of the basic crystal oscillator is higher than that of the L-C oscillator. However, if the required frequency deviation is in excess of the allowable crystal oscillator deviation, frequency multiplication has to be utilized. As is well known, multiplication reduces the coherence time by the square of the multiplication factor p, or

$$\tau_c^1 = \frac{\tau_c}{p^2} \qquad (2\text{-}12)$$

For a particular value of p the coherence time for both types of oscillators are equal. For the values given, this value is:

$$p_o = 24$$

With a multiplication factor of 24 the resulting frequency deviation of the crystal oscillator is $p_o \times n = 1/4\%$. It can be concluded that at the same frequency the crystal oscillator has a lower phase noise for deviations below 1/4%, while for deviations above 1/4% the L-C oscillator will have a lower phase noise.

2.1.8 AROD Implementation Considerations

An evaluation can now be made of several tracking loop configurations for the AROD system. The doppler frequency range is about 250 kc/s, required to track the carrier components. System errors should be less than 0.2 radians. The loop oscillator phase noise should be at least one order of magnitude lower, or less than 0.02 rad. rms. For a two-sided loop bandwidth of 200 cps, required to track high doppler rates with low dynamic errors, the minimum required coherence time can be calculated from equation (2-7):

$$\tau_c = \frac{\tau}{\phi_n^2} = 2 \text{ secs}$$

considerable care must be exercised in the design of the loop oscillator. In addition, the loop operating frequency (after multiplication) is typically 100 Mc/s, which makes the design of the loop mixer critical. It is therefore preferable to use the lowest possible basic frequency, using a "Q-spoiled" crystal oscillator and to use a minimum amount of frequency multiplication consistent with the required frequency deviation and phase noise limitations.

2.1.9 Notes on Long Term and Environmental Instabilities

Instabilities, other than short term, can be categorized into changes due to aging and changes with environmental fluctuations. Over short time intervals both effects can be neglected compared to the short term instability due to random noise. The only significance of the "external" instabilities is that it causes a shift in frequency or in frequency range of the oscillator. In particular, for the variable frequency oscillator, the shift of the frequency range can be undesirable if this shift is a larger percentage of the total range. Even though corrections can be made to cancel the aging effects, the design should minimize environmental instabilities.

Several observations can be made. The crystal oscillator, due to the stability of quartz, is inherently more stable than the L-C oscillator. However, if frequency multiplication has to be used to increase the frequency deviation, then the long-term and environmental instabilities increase with the factor of multiplication. It is possible, then, that with a certain multiplication factor the L-C oscillator can be used advantageously. Since a long term drift is identical to a doppler frequency offset in the AROD system, a drift is tolerable provided that the tracking filter loop gain is sufficiently high to minimize the error and sufficient dynamic range is available. For the AROD system, a long term drift of 50 kc/s is tolerable. For an L-C oscillator operating at 2.5 Mc/s the stability should then be 2%. For a crystal oscillator, which frequency has to be multiplied, the stability has to be 0.004%. It appears that neither system requires temperature stabilization, but may require periodic frequency adjustments.

2.2 Phase Locked Loop Experimental Investigation

Advanced circuit investigations have been made for the type I, second-order loop, using a voltage controlled oscillator mechanized with a varactor. Since there is no basic difference between a loop containing a pre-mixer and an internal IF section, and a loop without these elements, the investigation has concentrated on the simpler baseband loop approach. It contains a phase detector, a loop filter, a DC amplifier, and the variable oscillator. Consistent with the spaceborne application, efforts have been concentrated on employing circuits adaptable to integrated circuit technology in order to minimize size and weight requirements. This clearly indicates a preference for low operating frequencies.

In view of this and to avoid further system complexity with a consequent increase in circuit volume, an L-C type variable oscillator is attractive since it offers excellent phase noise characteristics at low frequencies, acceptable long term stability, and except for a small size coil of about 0.02 $inch^3$, can be readily integrated.

A phase locked loop is generally preceded by a hard limiter to present the phase detector with a constant level signal. Above a + 10 db input signal-to-noise ratio the phase detector gain is then a constant. At lower signal-to-noise ratios the gain decreases, causing a change in several loop parameters. In particular, the loop noise bandwidth decreases, partially offsetting the decrease in output signal-to-noise ratio. The limiter therefore performs as a form of self-adapting tracking aid, reducing the loop bandwidth when signal-to-noise ratio (and signal dynamics) is low and increasing the bandwidth for high signal levels, allowing higher doppler rates without loss of lock.

2.2.1 Limiter

The function of the limiter is to amplify the instantaneous value of the input signal level to a fixed output level while preserving its polarity, for all practical values of input levels. This can be achieved by sensing the

instantaneous polarity of the input signal in a crossover detector and by amplifying the detector output sufficiently to a saturation level.

In the limiter constructed and shown in Figure 2-3, crossover detection and saturation is combined in one network, a dual diode clipper. This is followed by a linear amplifier to obtain a high level, low impedance output. An advantage of this method is that the dual diode clipper has a crossover (phase) stability, independent of input level, which is then preserved in the linear amplifier. A saturating amplifier would generally not be phase stable with input drive variations, since storage time changes with level.

2.2.2 Phase Detector

The basic function of the phase detector is to produce a DC output voltage proportional to the phase difference of two signals of the same frequency. This can be accomplished in several ways and the selection of circuit configuration depends on such factors as operating input frequency, source and load impedances, input-to-input isolation, and ease of adapting to integrated circuit technology.

There are several basic configurations applicable to these requirements: a coincidence detector, a balanced mixer, and a half ring, as shown in Figure 2-4.

The coincidence detector consists of two crossover amplifiers, one for each input, connected to an AND gate, which produce an output only when both inputs are positive. The output of the AND gate is a periodic pulse train with a repetition frequency identical to the input frequency and a pulse width depending on the actual phase difference between the two input signals. After filtering of the r-f component the remaining DC component is a linear voltage representation of the input phase difference. The detector is immune to input level changes provided that sufficient drive is applied to the crossover amplifiers to cause complete limiting.

The balanced mixer type of phase detector is essentially a demodulator and usually consists of a full wave bridge or ring circuit with four diodes connected in symmetry. The output then is a product of the two input

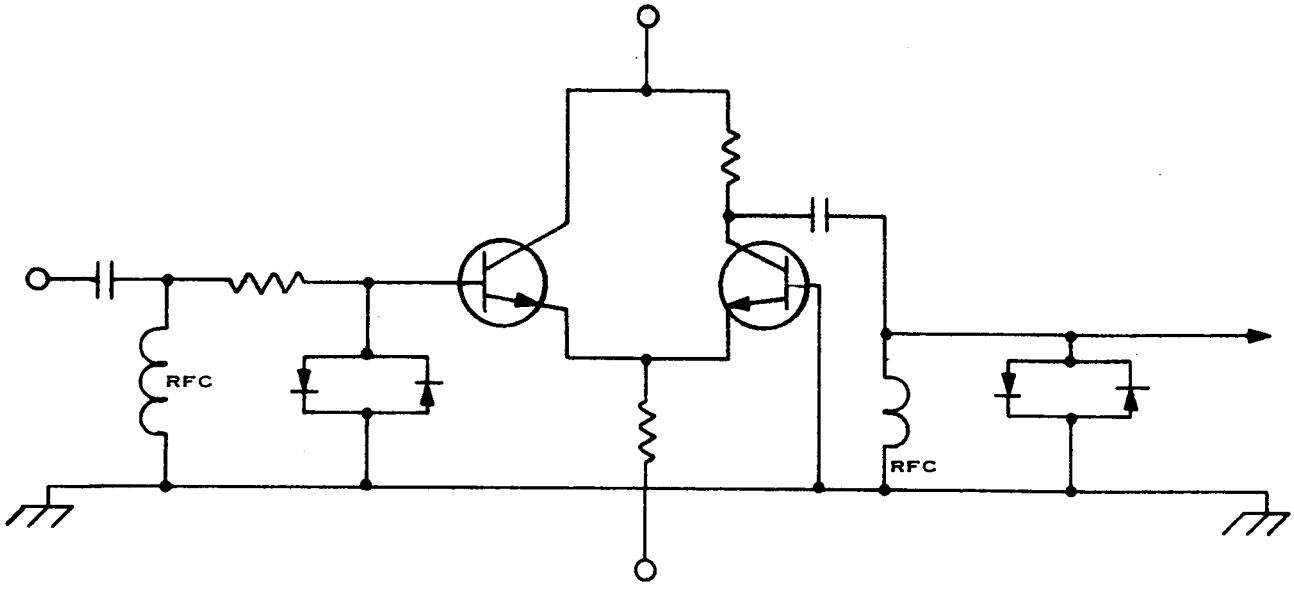
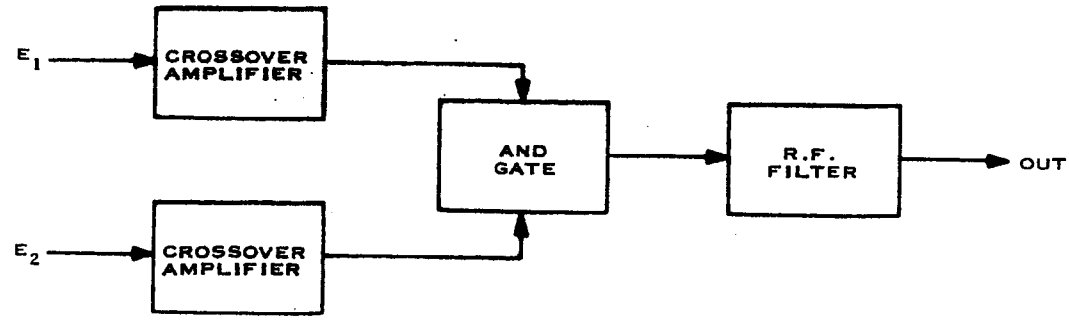
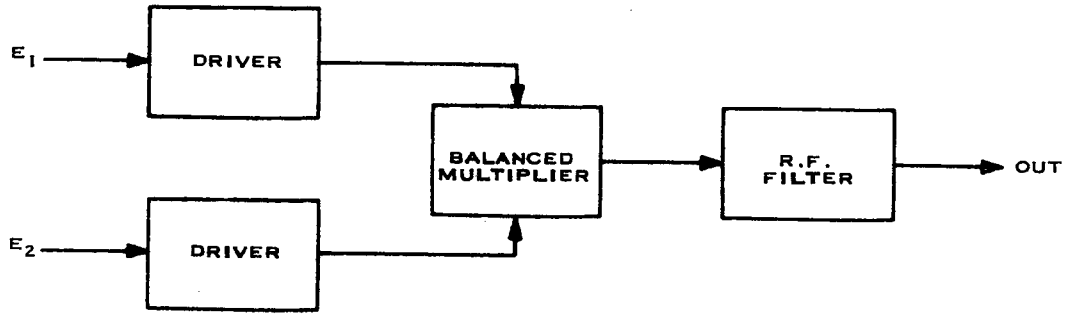


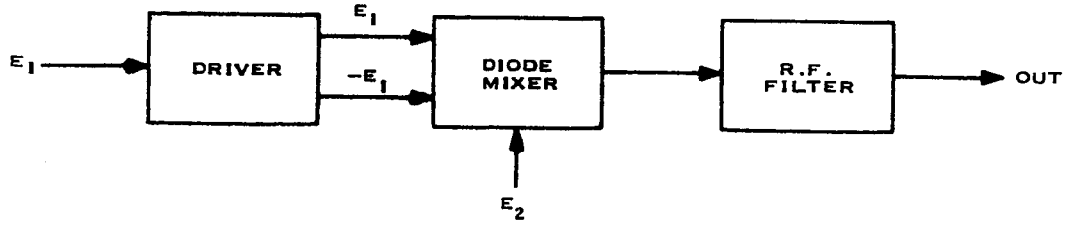
Figure 2-3. Phase Lock Loop Limiter



COINCIDENCE DETECTOR



BALANCED MIXER



HALF-RING DETECTOR

Figure 2-4. Phase Detectors

frequencies with a cancellation of the basic frequencies. The product, containing both sum and difference frequencies, is filtered to remove the r-f component. The resulting difference output, in the case of equal input frequencies, is a voltage representation of the input phase difference. With this circuit, however, the output is not a linear but rather a sinusoidal function of the input phase difference; it is also dependent on the input levels used. For a large difference in input levels the output is linearly dependent on the amplitude of the smallest input.

At a frequency of 1 to 5 Mc/s, either circuit could be used with good results. At higher frequencies the ring type demodulator is generally favored because of the difficulties involved in making an accurate and stable crossover amplifier at the short time intervals involved, while at lower frequencies the coincidence circuit is used because of the simplicity of that circuit and its operation.

A third type of phase detector has been investigated. Opposite phase signals from a single transistor drive a pair of diodes connected in series. The second r-f source is applied to the diodes' center connection, while the output is obtained from across the diodes. This circuit lacks in signal isolation, but since it avoids the use of transistors as crossover detectors and inductor elements, it is phase stable and lends itself readily to microelectronic techniques. This circuit will be used for L-C VFO and crystal VFO types of tracking loop.

2.2.3 Loop Filter

This part of the investigation has considered several filter configurations for a type I, second-order phase locked loop. For the specific AROD application a fairly high time constant is required, since the loop gain K must be high to minimize the static tracking error and the bandwidth must be low to obtain a large signal-to-noise enhancement. The time constant required will be in the order of 100 secs. This necessitates the use of a tantalum capacitor—specifically a solid tantalum for stability and reliability—with a very low leakage current. If a passive filter is used followed by a

DC amplifier, the input impedance of the amplifier must be very high. Together with the low drift requirements, the design of the amplifier becomes critical.

Another approach has been investigated. Using the inherently high input impedance of the varactor diode in the voltage controlled oscillator, the loop filter can be divided into two sections, one preceding and one following the amplifier, provided the product of the two transfer functions is equal to the required transfer function. The first filter, incorporated to prevent saturation of the DC amplifier, removes the major portion of the noise components and limits the DC voltage excursions to the amplifier to a certain extent. The second filter provides the required high time-constant to obtain the loop bandwidth.

This solution is acceptable for relatively low doppler rates. For high doppler rates the DC amplifier will saturate and the loop will lose track. Therefore, a third approach is being utilized in laboratory evaluation of loop performance. By making the loop filter part of an operational amplifier, the size of the filter components can be reduced, loading problems do not exist, and amplifier saturation cannot occur.

2.2.4 DC Amplifier

The low input levels and the high stability requirements indicate the necessity of either a chopper-stabilized or a differential amplifier. In view of the preferred loop filter configuration and because of simplicity, a differential amplifier has been chosen which can also be readily integrated. To make the loop parameters independent of the amplifier characteristics, a design with a very high gain is preferred. By using external feedback, the total gain can be set to the desired value, with an additional reduction in amplifier drift problems. Since the loop filter will also be incorporated in the feedback path, loop gain and response can be controlled by a single network.

Several such amplifiers are readily available on the market in both discrete component and integrated form. A Philbrick Research type P65A

operational amplifier is presently used for lab work. Output current capabilities are sufficient to drive the capacitive load (in the feedback path) for all applicable doppler rates in the AROD system.

2.2.5 Voltage Controlled Oscillator

As detailed in section 2.1 the phase noise of an L-C oscillator operating in the 1 to 5 Mc frequency range can be neglected, compared to the phase noise errors due to loop input noise. The long term and environmental drifts are less critical to the loop's performance. By designing the deviation range of the oscillator in excess of the required range, high drifts are tolerable. The system error due to a shift in nominal frequency is identical to the error incurred for a doppler offset and is equal to that offset in radians per second, divided by the total loop gain. Sufficient loop gain will therefore keep the drift errors within specifications.

The use of a varactor as the frequency control element will make the voltage vs frequency sensitivity curve nonlinear. The degree of nonlinearity depends on the varactor's control range and the amount of external capacity used in connection with the varactor, but is not objectionable for this type of phase locked loop application.

Phase noise measurements are generally taken by locking the unknown oscillator to a stable reference frequency in a phase locked loop, and by measuring the phase errors at the output of the phase detector. Coherence time can be calculated from this phase noise measurement and the loop bandwidth. An alternate method is to record the frequency of the locked unknown oscillator; and from the random frequency duration and the integration measurement time, the coherence time can again be calculated. Readability of frequency is increased in this method by mixing the unknown frequency with a reference that is several cycles removed from the unknown.

Since, for the AROD application, size and weight are of prime importance, the design of the oscillator has concentrated on the adaptability to integrated circuit techniques. With the exception of the inductor, this can

be accomplished and the overall oscillator size could be kept within 1/4 cubic inches. The circuit, as developed for the comparative evaluation measurement program, is shown in Figure 2-5. This represents a state-of-the-art L-C VFO implemented with varactor diode voltage control elements, low noise silicon transistors, and latest advances in powdered iron microminiature core inductors.

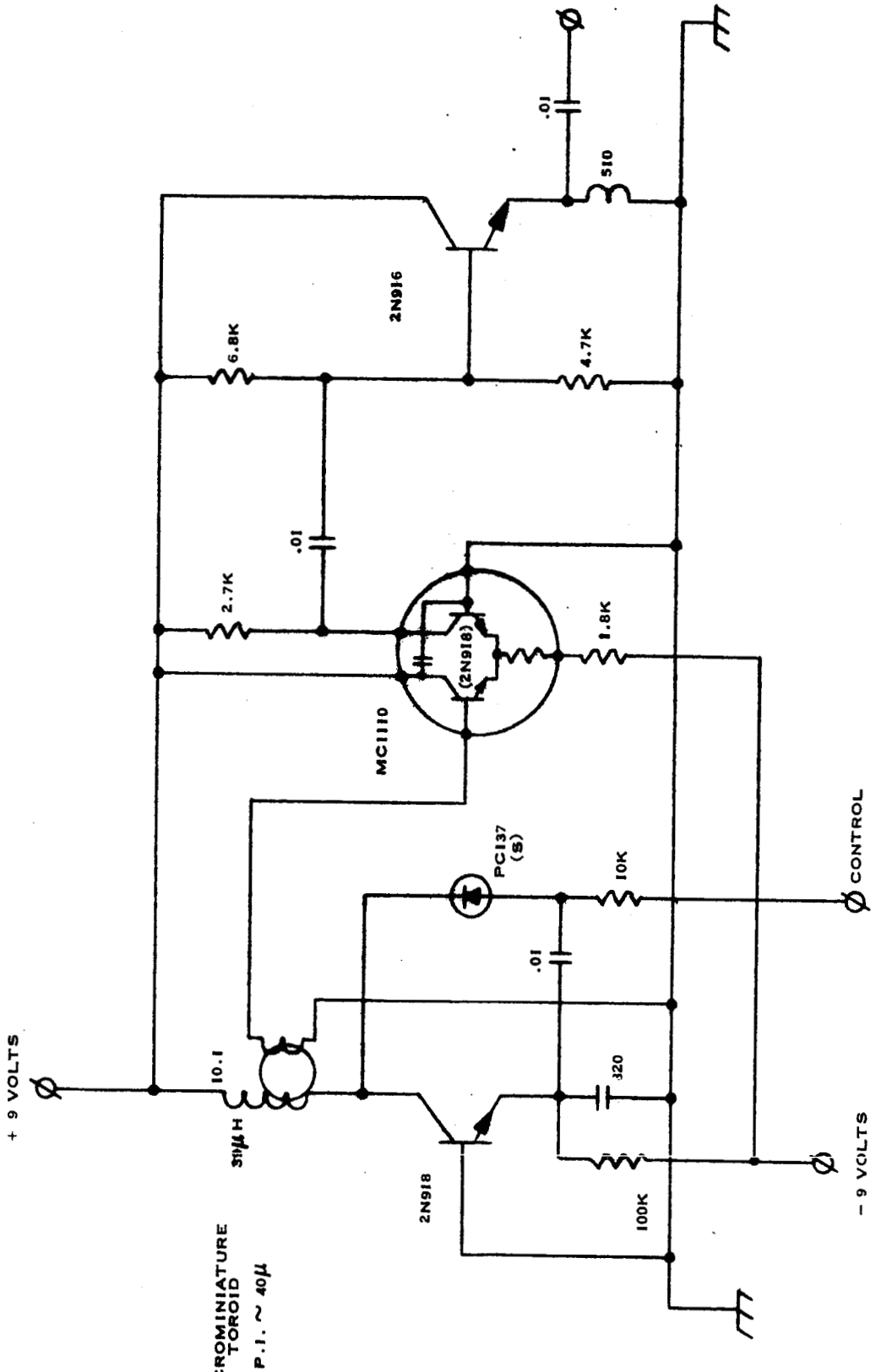


Figure 2-5. L-C Voltage Controlled Oscillator

2.3 State Controlled VFO's for Type II Phase Lock Loops

2.3.1 Type II Systems

The characteristics and problems of type II systems are well described in the literature[5] and will not be repeated here except with respect to the AROD tracking filter problem. The "type" designation stems from considering the number of integrations around the loop of a feedback control system. Thus, a type I has one integration while type II has two, and so on. At this point it is well to stress that the integrations being considered for purposes of this distincition are ideal, i.e., 1/s and not merely low pass filters with very low frequency corners. This will be discussed in depth at a later point. The essential performance difference between two systems of essentially equivalent relative and absolute stability, one type I and the other type II, relates to the steady-state errors encountered for various inputs. To borrow from servomechanism terminology, a velocity input would be followed with a finite position error (static error) for a type I system and a zero position error for a type II system.

The implications of this for phase lock loop (ϕLL) tracking filters of the AROD variety are of substantial importance. The first aspect concerns reacquisition after a signal fade, such as due to rocket flame attenuation, or for that matter, initial acquisition. The type I loop, when locked and tracking an input signal, acts in such a manner that the loop VFO may be characterized as a spring. The rest position of the spring corresponds to the center frequency of the VFO (usually a VCO). If the input frequency is different from the VCO center frequency a static phase error will exist in tracking similar to the force required to deflect a spring from its rest position. This simple analogy leads to two of the most important properties of a type I ϕLL from the AROD tracking filter application point of view. One is that the acquisition, or pull-in range, is finite (this follows intuitively from the spring analogy); and the other is that if lock is broken, the VCO returns to its "rest" center frequency (again the spring analogy).

A type II ϕLL, by virtue of the second integration (an "ideal" 1/s type it must be stressed), avoids both these shortcomings. Firstly, its initial acquisition range is theoretically infinite[6]; and secondly, when lock is broken the loop VFO will remain at the tracked frequency just before loss-of-lock, i.e., have a "memory," which is of course of inestimable value in establishing reacquisition. These desirable properties are a manifestation of the second integration which serves to eliminate the spring-like action encountered in a type I system. In addition, static phase errors are reduced to zero while dynamic phase errors, i.e., due to varying signal dynamics such as "acceleration," are dependent solely on how carefully the basic problem of applying type II systems is solved.

This basic problem pertains to the inherent instability of a type II system and the manner in which it is overcome by appropriate loop stabilization or equalization techniques. These techniques are all some form of phase lead compensation introduced via a series equalizer to realize a sufficiently long -1 slope roll-off in the vicinity of 0 db in the open loop transmission characteristic. If loop gain changes (for example, the usual change in phase detector gain with input SNR) are minimized, then the extent to which this equalization is required, and consequently the effect on closed loop bandwidth, can be controlled by design to meet loop phase margin requirements.[5]

The manner of implementing this integration and its relation to the integration implied in a type I loop will now be discussed. The physical basis of the integration action encountered in a ϕLL is the act of feeding back to the loop comparator the output quantity phase, while the controlled variable output is a frequency. That is to say the frequency, which is $d\phi/dt$ (the rate of change of phase with time), is integrated by the feedback (or H) block, which is an ideal 1/s, to yield phase. Note that this integration, while existing functionally in a block diagram representation, is not physically implemented in any way. Furthermore, the process is ideal, i.e., no low frequency corners exist as do in any physically realizable signal integrator. This provides a convenient basis of distinction between different methods

of achieving integration. A signal integrator is one which integrates a signal quantity, e.g., a voltage or current, to yield another signal quantity (voltage or current). A state integrator, on the other hand, involves a signal quantity (voltage, current or shaft velocity, for example) as the input and a state quantity (magnetic flux, electric displacement or shaft position, respectively) as the output. State integrators are inherently ideal in their 1/s nature, such as phase is the integral of frequency, position is the integral of velocity, change is the integral of current ($i = dq/dt$), or for that matter Faraday's Law ($e = d\Psi/dt$). Conversely, signal integrators, such as a passive RC networks or sophisticated operational amplifier type integrators, are never ideal by their very nature.

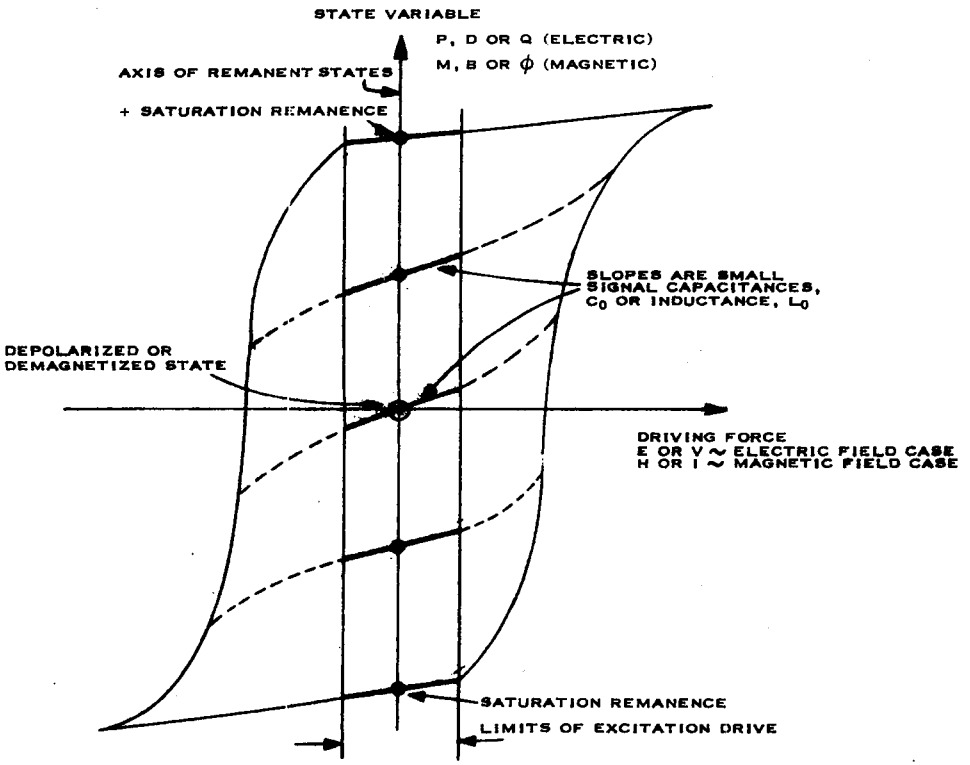
The foregoing distinction is very important with respect to realization of the benefits which a type II approach should provide. If the second integration (in addition to the ideal state integration of frequency to phase as already discussed) is implemented as a signal integrator with some characteristic low frequency corner, then the features of very broad acquisition range and loop memory (supposedly characterizing a type II approach) will not be achieved. For example, a one-second memory suitable for reacquisition would require an integrator with a corner as low as 0.25 Hz. The difficulties of implementing such an integrator with passive RC techniques, or even non-chopper stablized operational techniques, are obvious. For a corner this low the acquisition range will have contracted such as to be not very much larger than a second order type I loop[6] while the "memory" is clearly less than the 15 seconds which may be a significant AROD requirement. To summarize then, the attendant advantages of a type II approach are clearly dependent on implementing a second state (or ideal 1/s) integration within the loop. One manner of achieving this will be discussed next.

2.3.2 Nature of State Control for an L-C Oscillator

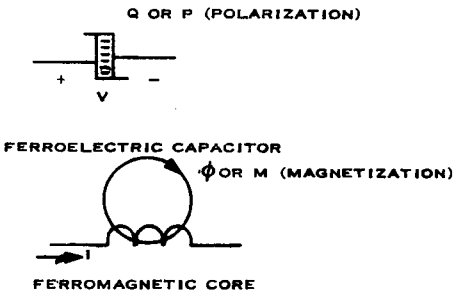
The most likely place to achieve a second integration of the state variety is the loop VFO. A typical example of a state controlled L-C variable frequency oscillator is the usual tuning condenser control of an oscillator,

such as encountered in signal generators. In this example the state which determines oscillator frequency is the rotational position of the condenser shaft. This is in contrast with the action of a voltage controlled oscillator (VCO) type VFO in which the oscillator frequency is determined by a voltage (i.e., a signal) acting on a suitable voltage controlled reactance in the oscillator tank. A solid-state approach to achieving a VFO with characteristics similar to the tuning condenser approach will require implementation of one or both of the L-C tank elements of an oscillator circuit by a suitable nonlinear reactance. Varactor diodes are excludable from this category in that a steady voltage is required to change and maintain a variation in small-signal capacitance. If the DC voltage is removed, then the charge stored on the large-signal capacitance of the diode will momentarily maintain the operating point. However, with the passage of time this will gradually shift as the charge leaks away through various diode imperfections. This is a consequence of the fact that the control of the device parameter sought after is established by stored energy—not by a state. To maintain the stored energy in such a device, a signal variable, such as voltage or current, must be continuously applied. On the other hand, a state control of the device parameter requires a signal variable only to effect changes in state.

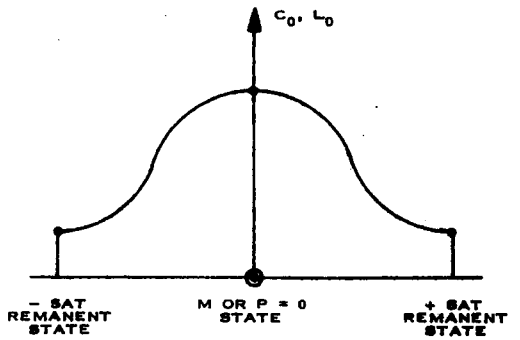
A class of devices which exhibits this action is based on the hysteretic properties of certain ferromagnetic and ferroelectric materials.[7,8] The large- and small-signal characterization of "inductive" and "capacitive" circuit elements based on such material properties is depicted in Figure 2-6 in a generalized manner for both electric and magnetic field phenomena. The large-signal characteristic is the commonly encountered hysteresis loop shown in Figure 2-6. When small-signal operation (as depicted by the limits shown on Figure 2-6a) is maintained, then characteristics such as shown on Figure 2-6c are obtained for the circuit elements indicated on Figure 2-6b (with appropriate variable identification). The important point is that the remanent state determines or controls the small-signal properties. Note that an infinity of remanent (i.e., driving force zero) states exists between the two saturation remanent states. In general,



A.) LARGE - SIGNAL CHARACTERISTICS



B.) CIRCUIT ELEMENTS



C.) SMALL - SIGNAL PROPERTIES

Figure 2-6 General Characterization of Nonlinear Reactive Elements

nonlinear reactance elements of this type are not characterized as having good long-term stability of their small-signal parameters. However, for the AROD ϕLL tracking filter requirement, this is not particularly important.

The implementation of these material properties in devices exists as ferroelectric capacitor elements and ferrite cores having single or multiple apertures. The ferroelectric materials are generally of the barium titanate class[8] and may be fabricated into "capacitor" elements from either single-crystal or polycrystalline materials. The saturation polarization for physically small elements is of the order of several microcoulombs. Since a polarization change from saturation remanence to the depolarized state (see Figure 2-6a) is a transfer of charge—and charge is the time integral of current, then the order of microamperes of current is required to effect such a state change in about a second. Note that an integration is intrinsically involved in such a state change. For a ferroelectric capacitor the limits of excitation drive for small-signal operation (as shown on Figure 2-6a) are established by a parameter termed the coercive electric field, which is a material parameter. On a device basis, this parameter appears as a coercive voltage, and is typically anywhere from 4 to 25 volts depending upon fabrication. A newer material type is the ferrielectric class developed by Prof. Pulvari at Catholic University.[9] These materials have excellent electrical and physical properties, such as Curie temperature[5,6] greater than $+300^{o}C$. They are characterized as MBO (mixed bismuth oxide) type ferrielectrics and are available commercially as single-crystal "capacitor" elements from Electrocristal Corp. The measured properties of AROD VFO applicable resonators based on polycrystal type devices will be presented later. The single-crystal types are expected to exceed these observed properties by at least an order of magnitude.

The other class of state-controlled nonlinear reactance elements are magnetic in nature and are consequently duals of all effects observed in the electric field class. This particular point makes this class somewhat less

desirable than the ferroelectric capacitor. Note that current was integrated to charge and consequently polarization state for the "capacitor" case. For equivalent action in the "inductor" case a voltage must be integrated to flux and a corresponding magnetization state change. In solid-state circuitry high impedance current sources are much easier to develop than equivalently low impedance voltage sources largely due to the fundamental current control nature of transistor devices.

To operate a small single-aperture core device from a voltage source would require source impedances below the micro-ohm level—which is quite impractical. Note that operation from a current source would negate the desired state control action completely. However, such "integration" action has been obtained[10] under suitable conditions for a very limited scope of application totally unsuited to the AROD VFO requirement. A more satisfactory approach to achieving action equivalent to state control from a voltage type signal source is the use of multi-aperture cores (sometimes termed transfluxors).[11] While the action thus obtained is not as determinate as the exact integration encountered with the ferroelectric capacitor approach, the multi-aperture core element is deemed worthy of continued investigation as a backup to the preferred method. Resonator characteristics for both will be subject to continuing investigation as a basic input to the entire problem of implementing an AROD-suitable, state controlled VFO.

At this point it may be well to summarize some of the pertinent aspects of state control insofar as it influences the action of a ϕLL implemented with such a VFO. First note that the "spring" action is entirely absent as a consequence of the device's dielectric material property of multi-state remanence. That is to say that an oscillator's frequency does not have any preferential state, but is free to exist at any value as defined by the parameter variation range as shown in Figure 2-6c. In addition, the "memory" is perfect and is in fact a non-destructive readout (NDRO) storage element (to use computer parlance). Secondly, the input variable to be integrated

must always be the signal variable dual of whichever variable constitutes the driving force (i.e., current input if the driving force is voltage) if state control action is to be obtained.

2.3.3 Resonator Characteristics

The application of the preceding concepts to an L-C VFO is considered most promising. While fundamentally amenable to controlling a crystal oscillator, certain difficulties with parameter value ranges and Q's make such application less promising. Also, the fact that long-term stability is not of fundamental importance makes the limited deviation range of a crystal and the concomitant need for frequency multiplication unattractive for this application. The key factors are adequate deviation range, greater than 200 Kc, with sufficiently high Q to reduce oscillator phase noise[2] to acceptable limits. Another factor of considerable application performance for the AROD vehicle tracking filters is amenability and compatibility with integrated circuit technologies. This problem is particularly severe with respect to the inductance [12, 13] element of the oscillator resonator. Inductance elements are completely incompatible with either monolithic diffused or thin-film microcircuit technologies, due to the conflict between a planar geometry and the solenoidal geometry desired. Consequently, the only realistic path is amenability to IC technology, i.e., small size and convenient interconnection characteristics. The inherent difficulty with this approach is the Q. As inductors (energy storage in this context) are made smaller in all dimensions, their Q's drop drastically because of the limit imposed by the conductivity of copper[13]. To some extent then, low resonator Q must be lived with in an overall oscillator design. This low Q will be caused by the inductor whether it is functioning as the linear element or the state control nonlinear reactance element.

For the linear element function a toroidal structure is desirable because of high magnetic "efficiency" or effectiveness. This rules out ferrite or metallic tape materials since they are homogenous and thus not suited for predictable inductance parameter energy storage applications. Some form

of "gapping" is required to stabilize the intrinsic material variations. The most satisfactory approach is some form of distributed air-gap pressed powder ("dust") core in a toroidal configuration. In the 1 to 5 MHZ frequency range, which appears most likely for implementing the AROD tracking filters, a carbonyl iron type offers the right balance between μ and Q and a sufficiently high μQ product. Until very recently these cores were not available in microminiature toroidal sizes. Work at Arnold Engineering Co. has led to such toroids down to 110 mils in O.D. Samples received have been used to fabricate inductors with L's over 5μH with Q's greater than 50. This constitutes respectable performance from the point of view of both electrical and performance size.

Resonators based on both ferroelectric capacitors and multi-aperture ferrite core devices have been constructed and investigated in the 1 to 5 MHZ frequency range at impedance levels commensurate with good transistor LC oscillator design approaches. The capacitors were procured from Waddell Dynamics and are of the polycrystalline ceramic type (trade name: Ceraelectric or Ceracaps) ferroelectrics. A wide range of nominal parameters were measured for Q's and deviation range of the resonator's resonant frequency. The instrumentation of Q was the current dual of the usual voltage-driven series resonator approach of most Q meters. This permitted simple accurate measurement for Q's greater than 10 by using a Tektronix P6016/131 current probe measuring tank and line currents as shown on Figures 2-7 and 2-8. Note that the manufacturer's specified values are quite meaningless as far as small signal characteristics are concerned.

Figure 2-7 shows that Q's are less than satisfactory for this application. However, effective resonator Q may be improved to the extent that a linear capacitance may be shunted across the ferroelectric capacitor at the expense of reduced frequency deviation. The curves of Figure 2-8 show adequate deviation capability, e.g., 250 KHz at 2.5 MHz, but not sufficient for "padding." The ferrielectric units expected from Electrocristal appear, from the basis of preliminary examination of a sample, to have Q's of greater than 80 and deviation capabilities of 2 or 3 to 1. That is, the small

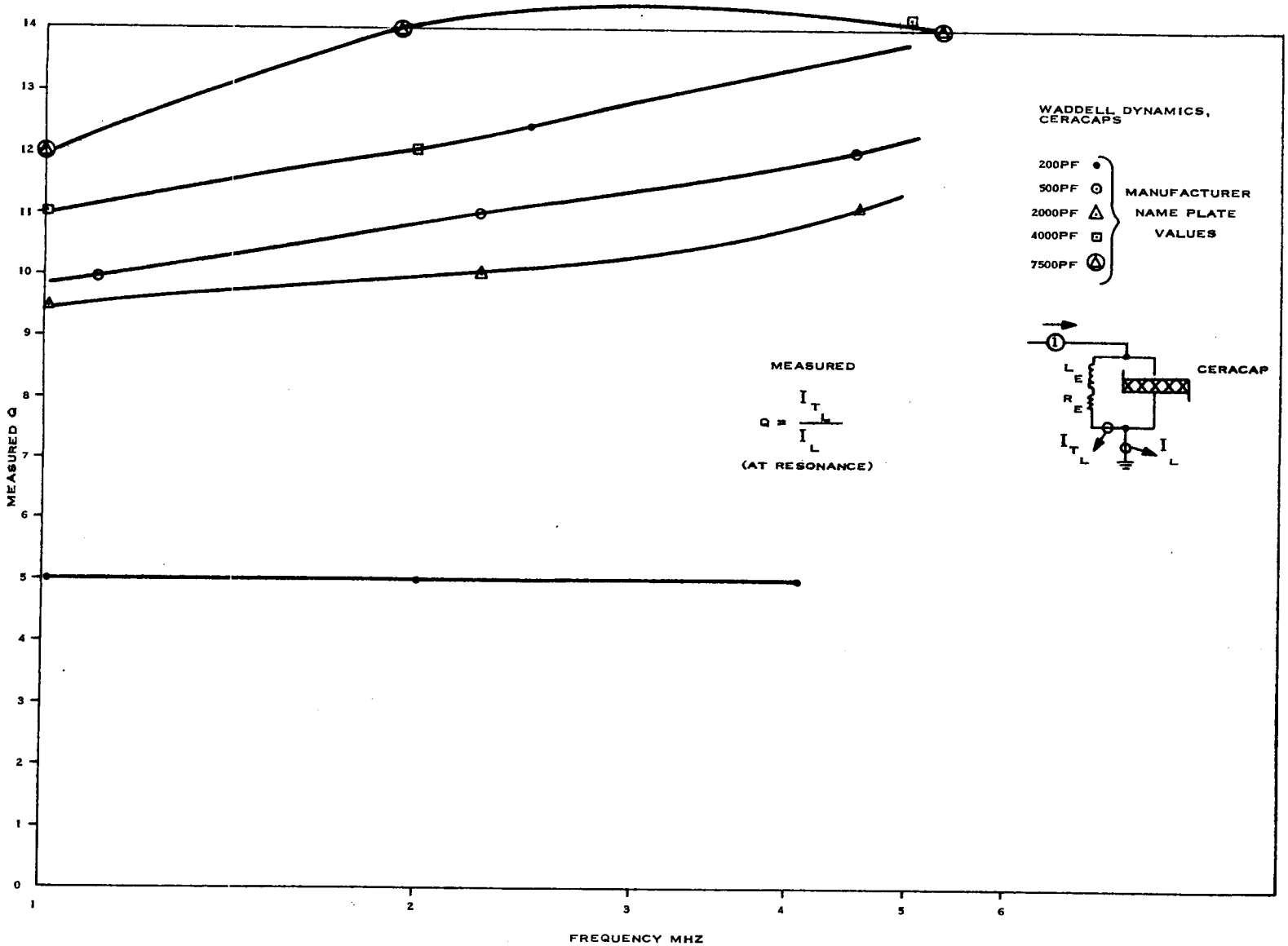


Figure 2-7 Ferroelectric Capacitor "Q" vs Tank Resonant Frequency

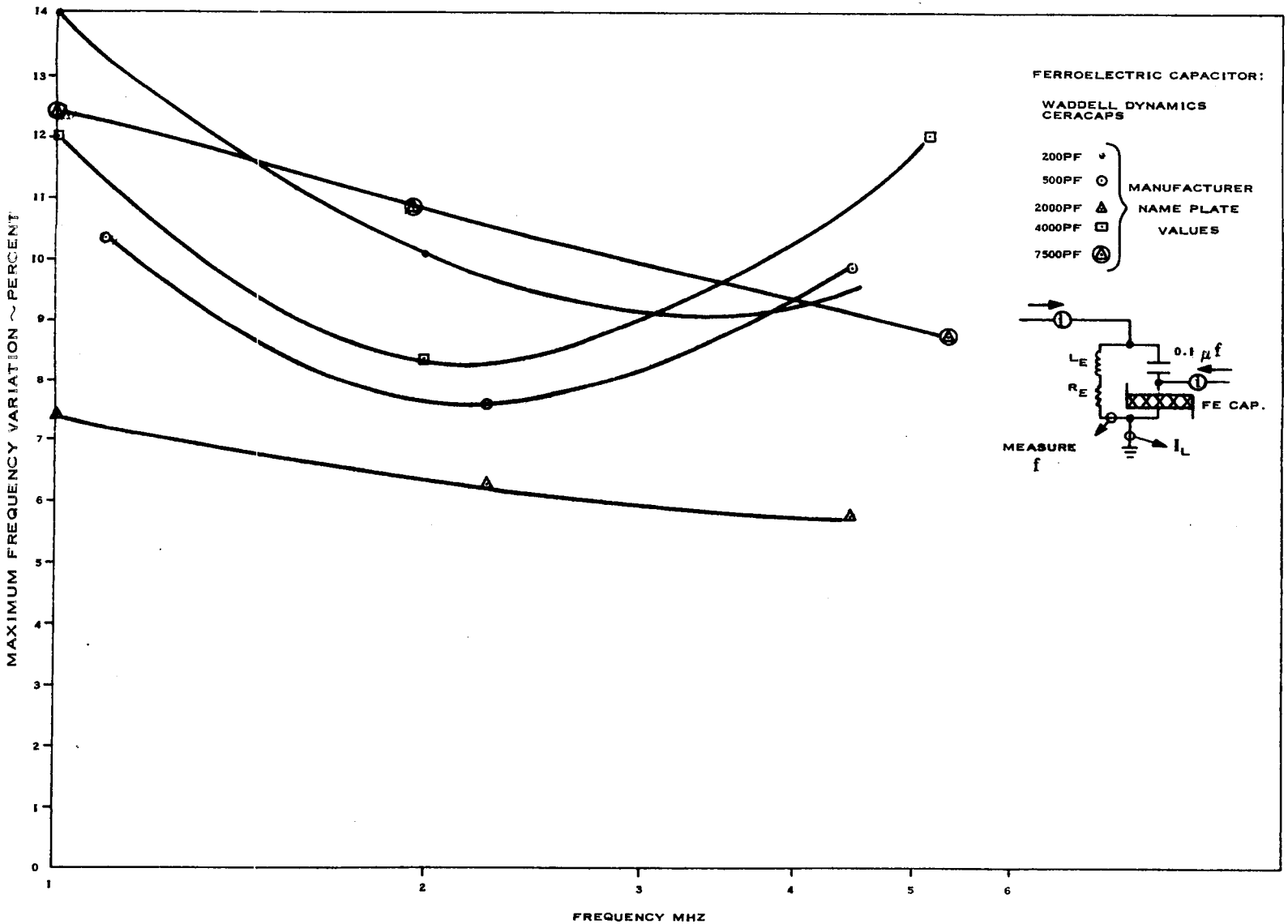


Figure 2-8 Maximum Variation of Resonant Frequency vs Tank Resonant Frequency

signal capacitance parameter changes by a factor of 4 or more, depending on excitation drive limits. The Waddell Ceracaps have been used however to implement a VFO as discussed in section 2.3.4. Further negotiations are being conducted with the manufacturer to see what improvements can be made in Q's and deviation range, or both. Preliminary discussion seems to indicate that these units are characterized in a large-signal "switching" manner by the manufacturer as far as process technology and test specifications are concerned. Improvements in process associated with the ceramic technology may possibly lead to large-scale improvements in Q. The present results with the Ceracaps are sufficient for the moment to investigate their use in a state controlled VFO with a somewhat reduced frequency deviation in order to improve Q by "padding" with high Q linear C's. The basis for permissible use of rather low Q's will be discussed in section 2.3.4.

Several sample multi-aperture ferromagnetic core devices were briefly examined for suitability for these purposes. Unfortunately, some rather inconveniently large devices exhibited good characteristics, but their large diameter of over 300 mils and thickness of 100 mils made them quite unsuited for incorporation into a design approach which had IC technology as its ultimate goal. On this basis a five-aperture core, the General Ceramics F-1023, in three basically different material types was investigated. Values of Q and L_e, R_e were measured in the same parallel resonator configuration and technique as employed for the ferroelectric capacitors. The data is presented for the frequency range of interest in Figures 2-9 and 2-10. Note that a unity permeability sample (a similar sized element except fabricated of phenolic) was included to establish a basis for separation of Q degradation effects between core and copper loss causes. The S3 type material appears to offer the best combination. It should be noted that this core is essentially 160 mils max OD and 50 mils thick. It appears that a slightly larger size would improve properties considerably. Samples of such a core in S3 material are being awaited for evaluation. The status of the core investigation will remain a backup until the ferroelectric (or, ferrielectric)

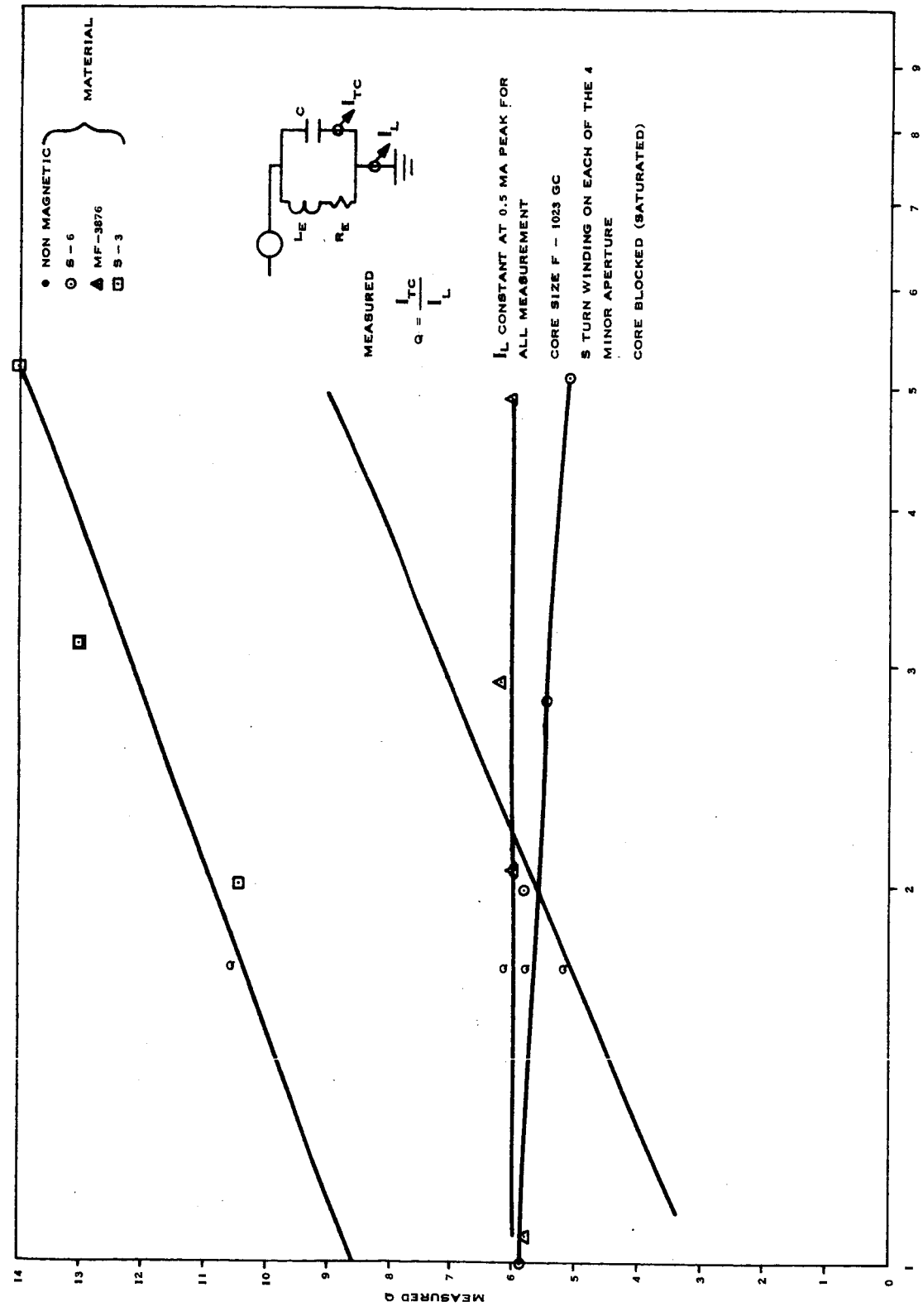


Figure 2-9 Multiaperture Core "Q" vs Tank Resonant Frequency

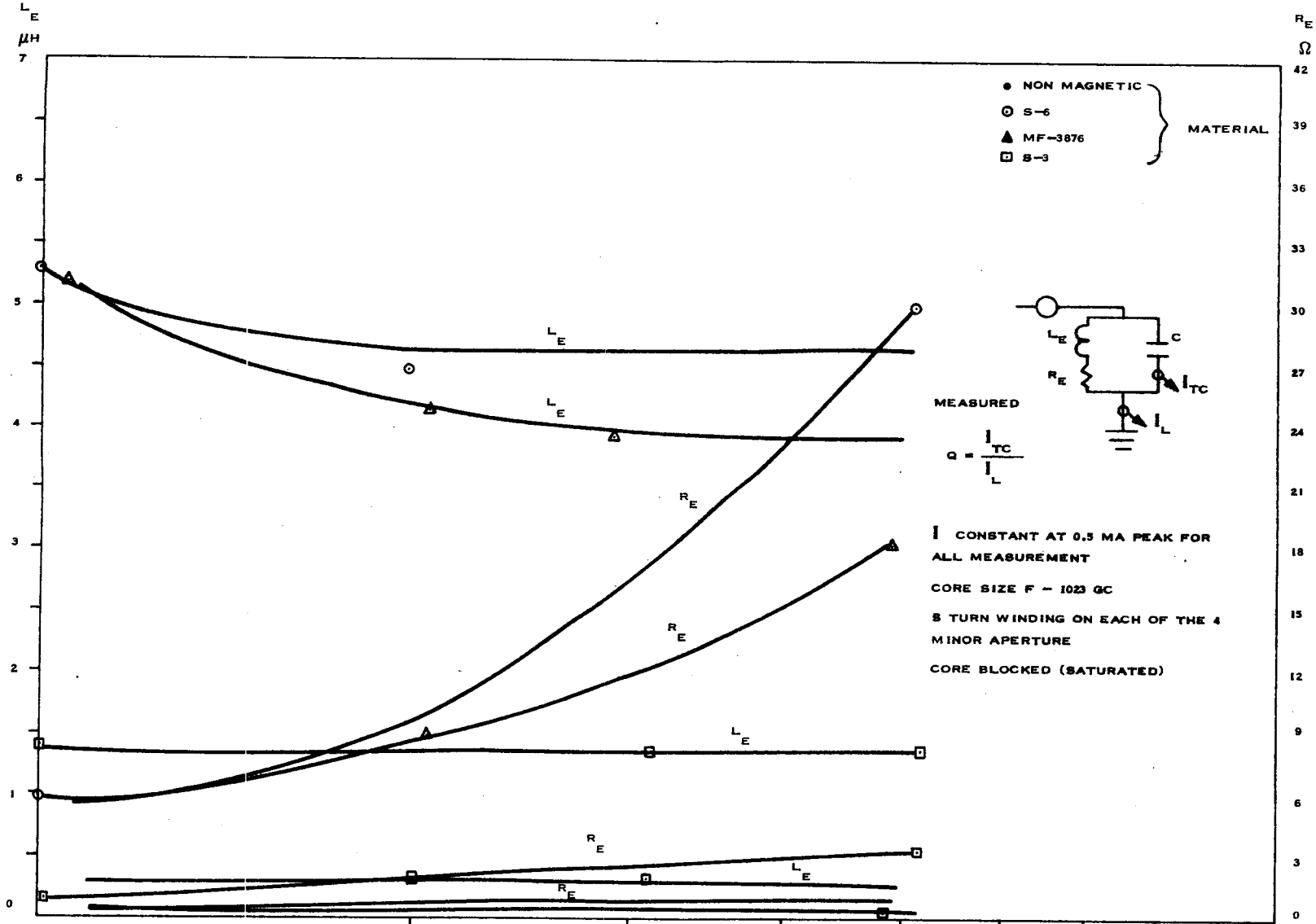


Figure 2-10 Multiaperture Core L_e, R_e vs Tank Resonant Frequency

capacitor approach (which is strongly favored for a variety of previously discussed reasons) no longer appears feasible in terms of sufficient Q and deviation in sufficient combination.

2.3.4 VFO-Multiplier (Phase Detector) Circuit Development

Various configurations for a state controlled L-C oscillator based on Colpitts/Clapp design, using either the "inductive" or "capacitive" nonlinear reactance element, were examined in considerable detail. However, the early realization of the inevitability of relatively low resonator Q's, regardless of which approach to the state controlled reactance chosen, forced a revision in thinking. Edson's work on oscillator phase noise indicates the obvious desirability of high Q since it appears as a squared term in the expression for coherence time.[2] However, in lieu of high Q, one can manipulate the P (resonator active power term) and S factors (which considers oscillator circuit non-linearities) to a large degree. There appears to be no fundamental difficulty in arriving at resonator powers of the order of 50 MW without departing from the small-signal region of either the two types of nonlinear reactance elements under consideration. This is in marked contrast to the design problem encountered with p-n junction type capacitance varactors, which operate at necessarily low powers for just such a reason. The degradation in coherence time represented by the S factor can be avoided by resorting to class A operation of the oscillator circuit in all respects.

This can be readily achieved by a simple ALC (AGC) loop and avoiding the loading of the oscillator directly by any nonlinear loads such as the ALC loop envelope detector. The requirement of AGC'ing transistor circuits has always been difficult to satisfy on a broad basis. The recent development of a hybrid integrated linear amplifier circuit (based on the use of two 2N918 prototype chips in what amounts to a differential amplifier configuration) has, among other very desirable properties, an extremely simple and direct gain control mechanism.[14,15] The technique is essentially an ideal multiplication of the Y_{21} gain (transadmittance) characteristic by

variation of the emitter current source. As such, the device is ideal for an ALC application to achieve a class A oscillator as well as implementing a multiplier for the loop phase detector function. However, to achieve the latter capability a slight change would be required on the MC1110, so that in the interim two matched 2N918's have been used—with less than optimum temperature characteristics of course.

The circuit for a state controlled VFO and multiplier type phase detector which has been developed is shown in Figure 2-11. The circuit employs only three microminiature (110 mil OD) powdered iron toroids in relatively low Q inductors and is well suited to hybrid integrated technology in terms of liberal use of transistors and permissible use of diffused capacitors. The ALC loop envelope detector is driven from the relatively broadband tuned amplifier buffer stage. This loop has sufficient "stiffness" to hold the oscillator resonator tank voltage to within 10 percent over the full deviation range. This successfully maintains operation of the ferroelectric capacitor in the small-signal region as well as avoiding nonlinear action of the oscillator transistor to reduce the effect of Edson's S factor on the coherence time. The multiplier stage, when hybrid chip integrated, will demonstrate low DC drift characteristics essentially equivalent to the 2N2060 class of dual differential amplifier transistor. Note that the 2N918's in this stage do not switch to a saturated ON condition, thus avoiding the long storage time difficulty inherent in such a non-gold-doped device.

The circuit as built performs satisfactorily and has been the subject of considerable bench optimization. It shows promise sufficient to justify extensive performance testing and measurement of various characteristics, such as phase detector gain change with varying input SNR's. The remaining work will completely characterize this circuit, subject to improvements in the state control reactance elements, and incorporate it in a type II ϕLL for performance measurement. Note from Figure 2-11 that all that remains for a type II implementation is the design of the DC (baseband) phase lead compensation network for loop stabilization and some nominal DC gain.

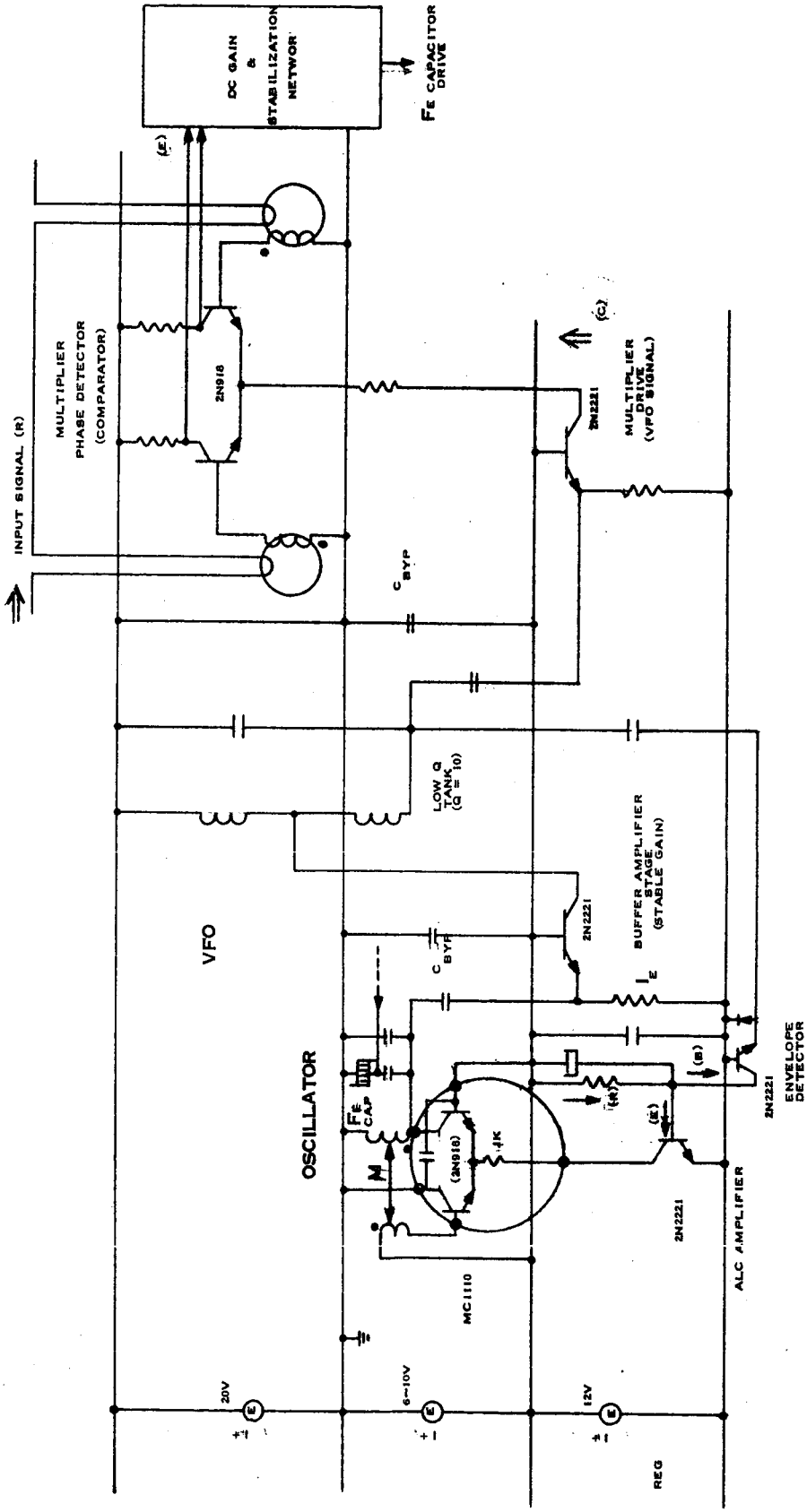


Figure 2-11 VFO—Multiplier for Type II ϕLL

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Section 3

LINEARIZED TRANSPONDER TRANSMITTER CHAIN

This section is an interim report by Maxson Electronics Corporation. on an investigation of one possible solution to the critical intermodulation problem inherent in effective SSB operation of the AROD ground station transponder transmitter. The technique involves envelope feedback around a wideband loop to linearize a triode cavity amplifier chain. The work is being carried out at L-band rather than S-band for reasons of component availability.

3.1 Purpose of Investigation

This report describes a simulated SSB two-tone test performed on an L-band cavity amplifier. The purpose of the program was to determine linear amplifier performance capabilities at microwave frequencies. The parameters for linear operation were to be determined. The intermodulation components of the two test signals were to be measured, and envelope feedback was to be employed to determine if significant improvement in the level of the intermodulation products could be achieved

Applications of linear amplifiers at lower frequencies, particularly for single sideband systems, have shown that the intermodulation distortion components are about 30 db below the carrier. Envelope feedback should be and is, in a properly designed system, capable of a 10 db improvement in the intermodulation levels and r-f feedback is capable of an additional 10 db of improvement. The purpose of the feedback is to reduce or prevent grid current, to prevent the amplifier from being operated at saturation levels, and to idealize the transfer characteristics.

For two equal amplitude signals the detected envelope has the shape of a full wave rectified signal. When passed through an amplifier which generates distortion the envelope of the detected output will differ from the input amplitude. If the output envelope can be matched to the input envelope the distortion will have been eliminated. The difference between the two envelopes is therefore used as an error signal to control the gain of the r-f stage to adjust the amplitude of the output envelope where it deviates (see Figure 3-1).

Maxson has developed several coaxial cavity amplifier chains operating at L-band for use in Tacan beacon systems. Envelope feedback for spectrum control has been employed in these amplifier chains with success. A Gaussian or high order cosine video reference pulse is compared with the envelope of the detected r-f pulse. The error signal is applied to the amplifier chain to correct the shape of the output envelope. The Tacan systems have a very severe spectrum control requirement. The video pulse is a pulse doublet with 3.5 microsecond half amplitude width and 12 microsecond spacing. It is required that the spectral energy in a 0.5 mc band centered 0.8 mc away from the carrier frequency be 60 db below the energy contained in the 0.5 mc band centered on the carrier frequency.

Several of these L-band cavity amplifiers were available and a test program was proposed to determine linearity performance under CW conditions. The program was limited to a six-week interval which precluded any extensive development of circuits. The intent was to use available laboratory instruments as elements of the equipment to be tested. The amplifier that was tested is the J1618 coaxial cavity made by RCA and designed for the 7651 tube. The 7651 is designed for pulse application. The 7650 is a CW version of the 7651 and has been used in SSB linear amplifiers at lower frequencies. It has the same physical dimensions as the 7651. Data supplied by RCA shows that at 30 mc the third-order distortion products were down at 31 db and the fifth order at 36 db. RCA does not have data as to the performance of these tube types as linear amplifiers at higher frequencies through the L-band. It is not known if any other organization has performed such tests. Both of these tube types were tested in

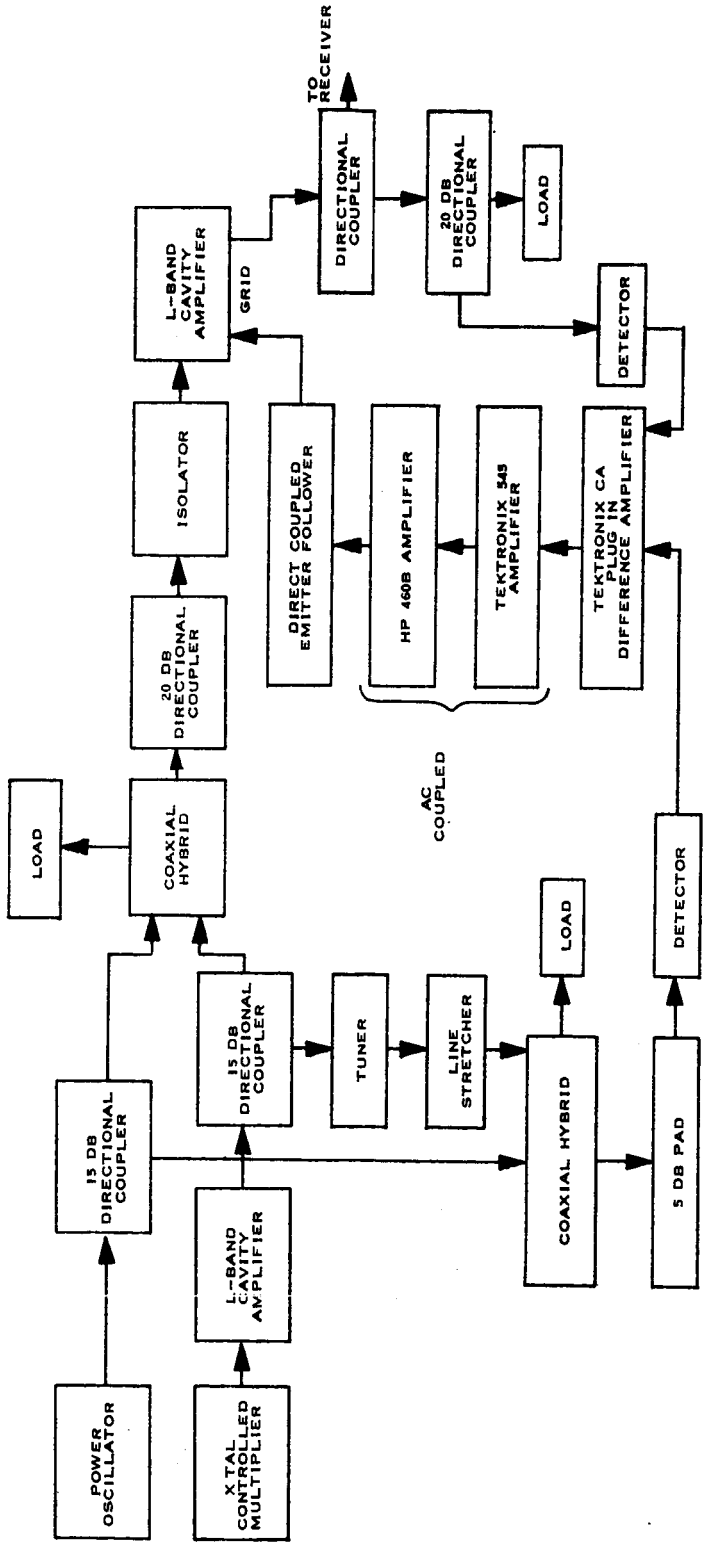

Figure 3-1 Linear Amplifier Two-Tone Test

the present program at 1160 and 1162.3 mc, the frequencies of the test tones. Other tubes will not be investigated due to the limited objectives of this program.

The experimental objective of the program was to demonstrate a linear amplifier with intermodulation components 40 db below the level of the test tones. This performance is to be obtained with envelope feedback contributing a 10 db reduction in the level of the intermodulation components. The test tones were to be separated by approximately 2.3 megacycles and of sufficient amplitude to generate 10 watts PEP out of the amplifier.

The intermodulation components were to be measured by using a narrow-band (10 kc) receiver as an r-f voltmeter (see Figure 3-2). The r-f signals are mixed down to the range of the receiver which has an attenuator at its input so that the receiver is operated at the same signal level input at all times. The difference in attenuator settings is the ratio of the intermodulation to main frequency levels. Receiver frequency differences are read on a EPUT counter with frequency converter by tapping off a portion of the receiver L.O. signal.

The theory of linear power amplifier design for minimum distortion and reliability is discussed by W. B. Bruene.* He presents an ideal tube transfer characteristic for zero distortion and shows that there is only one zero signal quiescent point where zero distortion will occur. A tube must be selected and placed into operation with these facts carefully considered.

A second paper by W. B. Bruene** discusses the envelope and r-f feedback techniques that have been employed to reduce distortion in single sideband transmitters. For envelope feedback the signal bandwidths and the feedback amplifier were in the audio range. The paper presents curves of performance with and without feedback for a 20 kw transmitter operating at a carrier frequency of 4 megacycles.

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* "Linear Power Amplifier Design," W. B. Bruene, Proc. IRE, Vol. 44, Dec. 1956, p. 1754.

** "Distortion Reducing Means for Single Sideband Transmitters," W. B. Bruene, Proc. IRE, Vol. 44, Dec. 1956, p. 1760.

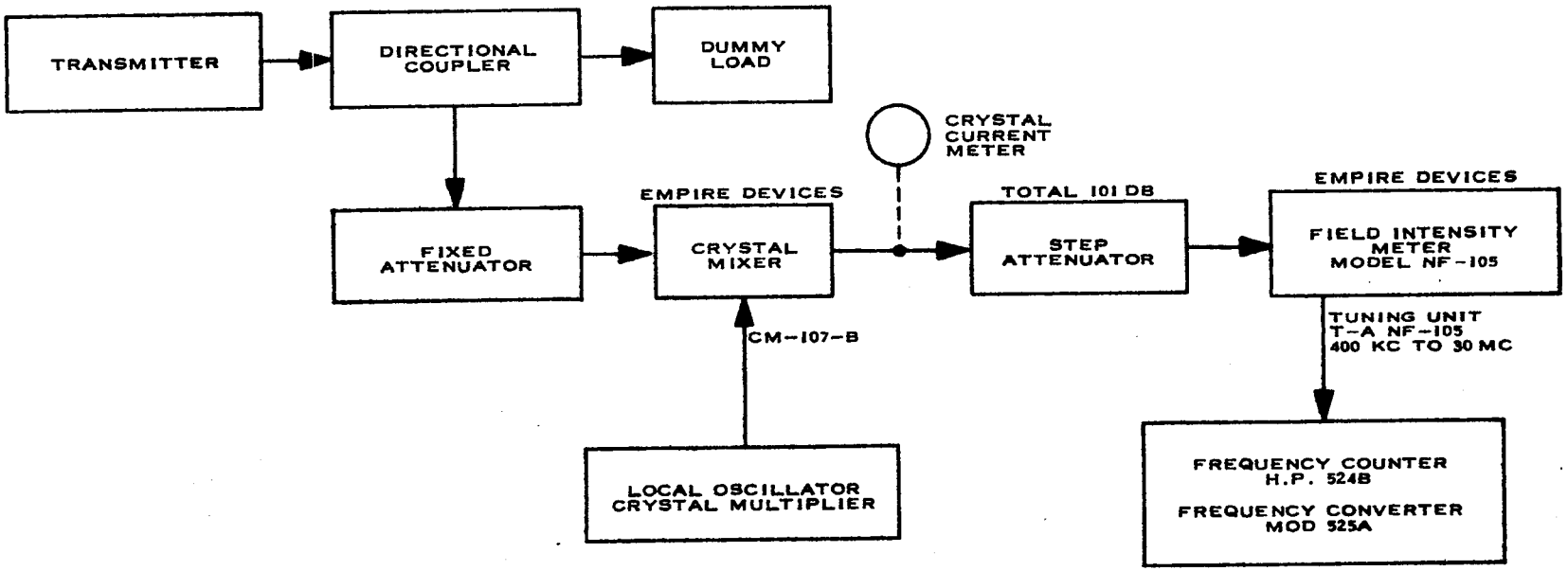

Figure 3-2. Measurement Technique

3.2 Results to Date

3.2.1 Open Loop Response

The first object of the program was to determine the open loop response. Characteristic curves of plate current vs grid bias for various screen voltages were measured. Performance of each tube was checked at a variety of operating points. The third-order components of 7651 could not be reduced below the 15 to 20 db region. The 7650 tube was substituted into the cavity and the remainder of performance tests were made with this tube.

With a properly selected bias point and the drive power adjusted so that grid current is not drawn during the peak of the envelope, the third-order intermodulation terms are down at 30 db and the fifth-order terms are down below -40 db. These values can be increased rapidly by changing the bias point or drawing grid current by increasing the drive power.

The 7650 was operated at average power output in the range of 5 to 10 watts and showed a gain of 6 db. The screen was operated between 200 and 600 volts at average plate currents with drive power of 200 to 300 ma. With the plate voltage at 1500 to 2 kv the resulting efficiency is quite low. This should not be considered as typical for the class of tube. No attempt was made to determine the effect of plate voltage on the power output and intermodulation components. The tubes are designed for high plate voltage and high peak current performance.

3.2.2 Feedback Loop

Video detectors were employed to obtain the envelopes of the input and output waveforms of the amplifier. The detectors were d-c biased to put them into linear regions.

A Tektronix 545 oscilloscope with type CA plug-in was used to obtain the error signal and provide broadband gain. The error signal was taken from the vertical output and further amplified in a H. P. 460B broadband amplifier. The amplifier has a gain of 15 db.

The grid network of the J1618 cavity has an input capacity of 300 picofarads. A dual emitter follower was constructed to drive this capacity.

Open loop frequency response of the feedback loop extended beyond 15 megacycles.

With the feedback loop closed, a 5 db improvement in the level of the third-order modulation components could be obtained with only 0.5 db reduction in power output. The open loop intermodulation components are at 20 db for this closed loop performance. The feedback loop improvement decreases as the open loop intermodulation level is reduced.

3.2.3 Factors Affecting Performance

1. The r-f cavity has a bandpass of 4 megacycles. The two input frequencies spaced by 2.3 megacycles experience a relative phase shift in passing through the cavity. The result is an envelope delay of about 60 nanoseconds. A compensating delay was introduced into the reference channel so as to obtain a correct error signal, but the error signal is applied late.

The phase delay must be minimized by using a circuit whose bandpass is as broad as possible, relative to the frequency separation of the two input frequencies.

2. The feedback loop, as it was instrumented was an a-c loop. The amplified error signal has an average value when a-c coupled such that positive going portions of the error signal are more positive than the bias level and thus behaving as positive feedback rather than negative feedback.

With the amplifier operated with low open loop distortion levels the maximum error occurs at the cusp of the detected envelope. The r-f tube gain must be controlled over the curved small signal portion of the grid characteristic. The cusps of the detected envelopes must be referenced to the same d-c potential for correct error generation and the d-c level must be passed by the feedback loop. This implies a d-c coupled broadband feedback amplifier or a combination of a-c and d-c feedback amplifiers to recover the d-c components.

3. The cusps of the video detected envelope generate high frequency components in the error signal which must be passed by the feedback amplifier. It has been suggested that the feedback path bandwidth requirement may be eased by employing homodyne detection for the reference and output signals. The error signal would more nearly be a sine wave with harmonic distortion components. After amplification the error could be converted to a unidirectional signal by using a phase splitter and recombining the two signals with the desired negative amplitudes.

3.3 Extension to S-Band

Amplifiers with greater percentage bandwidths can be constructed at higher frequencies. With larger bandwidth the differential phase delay is reduced. For example: For two tones with 2.3 mc spacing, passing through a 15 mc half-power bandwidth, the phase delay will correspond to an envelope shift of 17 nanoseconds. Delays due to cable length differences will also be reduced 2 to 1 by operating at S-band instead of L-band as in the present tests.

Representative of some S-band cavity amplifiers that are available, but not necessarily designed for linear amplifier service, are the following.

Resdel Engineering Corporation has a Model P-21H amplifier, operating in frequency range 2075 to 2325 mc. The amplifier has a 12 mc half-power bandwidth and 12 db of gain. It can generate 10 watts of cw power, operated class C at an overall efficiency of 33%.

Elimac has two cavities for operation in the 2200 to 2300 mc band. The characteristics of these two models are summarized in the table below.

	EM 4523	EM 4524
Power Output (Class A)	20 watts	80 watts
Drive Power	2	8
Bandwidth, 3 db points	10 mc	15 mc
Frequency Stability	20 PPM/^{o}C	20 PPM/^{o}C
Anode Voltage	750 v	1 kv
Anode Current	100 ma	250 ma
Plate Efficiency	26%	32%

How these amplfiers will perform as linear amplifiers is not known.

To apply feedback to cavities of this type will present no new problems. The feedback signal would be applied to either the cathode or the grid, depending on which element was available and of lowest capacity. Small, high current capacity transistor d-c modulators have been employed very successfully to cathode modulate RF tetrodes on our TACAN programs.